# SYLLABUS FOR M.TECH.

# (VLSI DESIGN & EMBEDDED SYSTEMS)

## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGG.

**SCHEME OF STUDIES & EXAMINATION**
**MASTER OF TECHNOLOGY(VLSI DESIGN & EMBEDDED SYSTEMS)**

**SEMESTER – I**

# EFFECTIVE FROM THE SESSION 2012-13

| Course No. | Course Title | Teaching Schedule | | | Marks | | | |
|---|---|---|---|---|---|---|---|---|
| | | L | T | P | Sessional | Exam. | Total | Duration of Exam |
| MT-VLES 501 | **IC Fabrication Technology** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES 503 | **Digital VLSI Design** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES 505 | **Hardware Description Languages** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES 507 | **Embedded System Design** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES 509 | **Signal Processing** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES -511 | **Digital VLSI Design Lab** | **-** | **-** | **3** | **50** | **50** | **100** | **3** |
| MT-VLES 513 | **Embedded System Design Lab** | **-** | **-** | **3** | **50** | **50** | **100** | **3** |
| **TOTAL** | | **20** | **-** | **6** | **350** | **600** | **950** | |

**SCHEME OF STUDIES & EXAMINATION**
**MASTER OF TECHNOLOGY (VLSI DESIGN & EMBEDDED SYSTEMS )**

**SEMESTER – 2**

# EFFECTIVE FROM THE SESSION 2012-13

| Course No. | Course Title | Teaching Schedule | | | Marks | | | |
|---|---|---|---|---|---|---|---|---|
| | | L | T | P | Sessional | Exam. | Total | Duration of Exam |
| MT-VLES 502 | **Analog IC Design** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES - 504 | **Embedded system Design-II** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES - 506 | **Low Power VLSI Design** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES - 508 | **Embedded system for Wireless & Mobile communication** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| | **Elective -I** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES - 510 | **Embedded system-II lab** | **-** | **-** | **3** | **50** | **50** | **100** | **3** |
| MT-VLES - 512 | **Analog IC Design Lab** | **-** | **-** | **3** | **50** | **50** | **100** | **3** |
| **TOTAL** | | **20** | **-** | **6** | **350** | **600** | **950** | |

**SCHEME OF STUDIES & EXAMINATION**
**MASTER OF TECHNOLOGY (VLSI DESIGN & EMBEDDED SYSTEMS)**

**SEMESTER -3**

# EFFECTIVE FROM THE SESSION 2012-13

| Course No. | Course Title | Teaching Schedule | | | Marks | | | |
|---|---|---|---|---|---|---|---|---|
| | | L | T | P | Sessional | Exam. | Total | Duration of Exam |
| MT-VLES -601 | **Adaptive Signal Processing** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES -603 | **Embedded Control system** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| | **Elective -II** | **4** | **-** | **-** | **50** | **100** | **150** | **3** |
| MT-VLES -605 | **Adaptive Signal Processing Lab** | **-** | **-** | **3** | **50** | **50** | **100** | **3** |
| MT-VLES -607 | **Seminar** | **-** | **-** | **2** | **50** | **-** | **50** | **-** |
| MT-VLES -609 | **Minor Project** | | | **4** | **100** | | **100** | |
| **TOTAL** | | **12** | **-** | **9** | **350** | **350** | **700** | |

**SCHEME OF STUDIES & EXAMINATION**
**MASTER OF TECHNOLOGY ( VLSI DESIGN & EMBEDDED SYSTEMS)**

**SEMESTER -4**

# EFFECTIVE FROM THE SESSION 2012-13

| Course No. | Course Title | Teaching Schedule | | | Marks | | |
|---|---|---|---|---|---|---|---|
| | | L | T | P | Sessional | Exam. | Total |
| MT-VLES -602 | **Dissertation** | - | - | 24 | 200 | 400 | 600 |
| **TOTAL** | | | - | 24 | 200 | 400 | 600 |

**M.D. University, Rohtak**
**Scheme of Studies & Examinations for**
**Master of Technology (VLSI DESIGN & EMBEDDED SYSTEMS)**

The Performance of the student of M.Tech shall be graded on the basis of percentage of marks and corresponding grades as mentioned below :

**A)**

| **Marks** | | **Grades** | | **Marks** |
|---|---|---|---|---|
| 85 | ≤ | $A_+$ | ≤ | 100 |
| 75 | ≤ | A | < | 85 |
| 60 | ≤ | B | < | 75 |
| 50 | ≤ | C | < | 60 |
| 40 | ≤ | D | < | 50 |
| 00 | ≤ | E | < | 40 |

| **Letter Grades** | **Performance** | **Division** |
|---|---|---|
| A+ | Excellent | First |
| A | Very Good | First |
| B | Good | First |
| C | Fair | Second |
| D | Pass | Third |
| E | Repeat | Fail |

**Note :** The Candidate who have passed all the semesters examination in the first attempt obtaining at the 75% marks in aggregate shall be declared to have passed in the first division with Distinction mentioned in the degree.

**B)**

Actual percentage of Marks Obtained and Corresponding grades should be mentioned on detailed marks certificate of student. To obtain 'D' grade a student must have secure at least 40% marks in each subject of the semester Examination.

**C)**

Student who earned an 'E' grade or less than 40% marks in any subject shall have to reappear in that subject.

# FIRST SEMESTER

MT-VLES **-501 IC Fabrication Technology**

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Environment for VLSI Technology** : Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.
**Impurity incorporation**: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterisation of Impurity profiles.
**Oxidation** : Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterisation of oxide films; High k and low k dielectrics for ULSI.
**Lithography** : Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.
**Chemical Vapour Deposition techniques** : CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and technology.
**Metal film deposition** : Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallisation schemes.
**Plasma and Rapid Thermal Processing**: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI.
Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

**Texts/References:**


1. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1994($2^{nd}$ Edition).
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
3. Plummer, Deal , Griffin “Silicon VLSI Technology: Fundamentals, Practice & Modeling” PH, 2001.
4. P. VanZant , “Microchip Fabrication”, $5^{th}$ Edition, MH , 2000.

MT-VLES **-503 Digital VLSI Design**

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Introduction to MOSFETs** : MOS Transistor Theory – Introduction MOS Device, Fabrication and Modeling , Body Effect, Noise Margin; Latch-up

**MOS Inverter** : MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Static Load MOS Inverters, Transistor Sizing, Static and Switching Characteristics; MOS Capacitor; Resistivity of **V**arious Layers.

**Symbolic and Physical Layout Systems** – MOS Layers Stick/Layout Diagrams; Layout Design Rules, Issues of Scaling, Scaling factor for device parameters.

Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.

Sequential MOS Logic Circuits: SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop.

Dynamic Logic Circuits; Basic principle, non ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

CMOS Subsystem Design: Semiconductor memories, memory chip organization, RAM Cells, dynamic memory cell.

**REFERENCE BOOKS**:


1. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits : Analysis and Design*, Third Edition, MH, 2002.
2. W. Wolf, *Modern VLSI Design : System on Chip*, Third Edition, PH/Pearson, 2002.
3. N. Weste, K. Eshraghian and M. J. S. Smith, *Principles of CMOS VLSI Design : A Systems Perspective*, Second Edition (Expanded), AW/Pearson, 2001.
4. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, *Digital Integrated Circuits : A Design Perspective*, Second Edition, PH/Pearson, 2003.
5. D. A. Pucknell and K. Eshraghian, *Basic VLSI Design : Systems and Circuits*, Third Edition, PHI, 1994.
6. J. P. Uyemura, *CMOS Logic Circuit Design*, Kluwer, 1999.
7. J. P. Uyemura, *Introduction to VLSI Circuits and System*, Wiley, 2002.
8. R. J. Baker, H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, PH, 1997.

MT-VLES **-505 Hardware Description Languages**

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Introduction To Hardware Design:** Digital System Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction.

**VHDL Background:** VHDL History, Existing Languages, VHDL Requirements, The VHDL Language.

**Design Methodology Based On VHDL:** Elements of VHDL, Top down Design, Top down Design with VHDL, Subprograms, Controller Description, VHDL Operators, Conventions and Syntax.

**Basic Concepts In VHDL:** Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.

**Design Organization and Parameterization:** Definition and Usage of Subprograms, Packaging Parts and Utilities, Design Parameterization, Design Configuration, Design Libraries.

**Utilities For High-Level Descriptions:** Type Declarations and Usage, VHDL Operators, Subprogram Parameter Types and Overloading, Other Types and Type Related Issues, Predefined Attributes, User Defined Attributes.

**Dataflow Descriptions In VHDL:** Multiplexing and Data Selection, State Machine Description, Three State Bussing.

**Behavioral Description of Hardware:** Process Statement, Assertion Statement, Sequential Wait Statements, Formatted ASCII I/O Operations, MSI Based Design.

**Verilog:** Overview of Digital design with Verilog HDL, Hierarchical modeling concepts, basic concepts, modules & ports.

**REFERENCE BOOKS**:


1. J. Bhasker, *A VHDL Primer*, Third Edition, PH/Pearson, 1999.
2. J. Bhasker, *A VHDL Synthesis Primer*, Second Edition, Star Galaxy, 1998.
3. J. Bhasker, *A Verilog HDL Primer*, Second Edition, Star Galaxy, 1999.
4. J. Bhasker, *A Verilog Synthesis : A Practical Primer*, Star Galaxy, 1998.
5. M. J. S. Smith, *Application Specific Integrated Circuits*, AW/Pearson, 1997.
6. Z. Navabi, *VHDL : Analysis and Modeling of Digital Systems*, Second Edition, MH, 1998..
7. J. Armstrong and F. G. Gray, *VHDL Design Representation and Synthesis*, Second Edition, PH/Pearson, 2000.
8. P. J. Ashenden, *The Designer's Guide to VHDL*, Second Edition, Morgan Kaufmann, 2001.
9. D. Naylor and S. Jones, *VHDL : A Logic Synthesis Approach*, Chapman & Hall, 1997.

MT-VLES **-507 Embedded System Design**

**L –T - P**
**4 – 0 - 0**

**Maximum marks:**100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Introduction to Embedded systems design:**
Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system, Use of target system or its emulator and In-circuit emulator, Use of software tools for development of an ES.

**8051 Microcontroller:** Microprocessor V/s Micro-controller, 8051 Microcontroller: General architecture; Memory organization; I/O pins, ports & circuits; Counters and Timers; Serial data input/output; Interrupts.

**8051 Instructions:** Addressing Modes, Instruction set: Data Move Operations, Logical Operations, Arithmetic Operations, Jump and Call Subroutine, Advanced Instructions.

**8051 Interfacing and Applications:** Interfacing External Memory, Keyboard and Display Devices: LED, 7-segment LED display, LCD.

**Advanced Microcontrollers:** Only brief general architecture of AVR, PIC and ARM microcontrollers; JTAG: Concept and Boundary Scan Architecture.

**REFERENCE BOOKS**:


1. Embedded Systems by Raj Kamal, TMH, 2006.
2. The 8051 Microcontroller by K Ayala, 3rd Ed., Thomson Delmar Learning, 2007.
3. 8051 Microcontroller by S. Ghoshal, Pearson Education, 2010.
4. The 8051 Microcontrollers by K. Uma Rao and A. Pallavi, Pearson Ed., 2009.
5. Microcontrollers by Raj Kamal, Pearson Education, 2005.
6. PIC Microcontroller by H.W Huang, Delmar CENGAGE Learning, 2007.
7. J B Peatman, Design with PIC Microcontrollers, Prentice Hall.

MT-VLES **-509 Signal Processing**

**L –T - P**
**4 – 0 – 0**

**Maximum marks:**100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Speech Processing :** Speech Communication Acoustic Theory of Speech: The Source–filter Model Speech Models and Features Linear Prediction Models of Speech Harmonic Plus Noise Model of Speech Fundamental Frequency (Pitch) Information Speech Coding, Speech Recognition

**Signal Processing and Auditory Perception:** Introduction , Musical Notes, Intervals and Scales Musical Instruments Review of Basic Physics of Sounds Music Signal Features and Models Anatomy of the Ear and the Hearing Process Psychoacoustics of Hearing ,Music Coding (Compression)

High Quality Audio Coding: MPEG Audio

**Time Delay Estimation:** Need for the Time Delay Estimation, System Model, Source Localization strategies,Ideal Model-Free field environment, TDE METHODS: Cross-correlation Function(CCF) method ,Least mean square (LMS) adaptive filter method ,Average square difference function (ASDF) method , Relation between the SNR level and the time delay estimation.

**Channel Equalization and Blind Deconvolution :**Introduction and need For Channel Equalization , Types of Equalization Techniques , Decision Feedback Equalization Non-blind Equalization Linear Equalization Blind Equalization General Mathematical Model , Channel Modeling and algorithms

. **System modeling and identification**: System identification based on FIR (MA), All Pole (AR), Pole Zero (ARMA) system models, Least square linear prediction filter, FIR least squares inverse filter, predictive de convolution, Matrix formulation for least squares estimation: Cholesky decomposition, LDU decomposition, QRD decomposition, Grahm V Schmidt orthogonalization.

**REFERENCE BOOKS**:

1. Siomon S Haykins, “Adaptive Filter Theory,”PHI, 3rd Edition
2. Proakis,”Digital Signal Processing,”PHI 2nd edition
3. Harry L. Van Trees, “

## MT-VLES -511DIGITAL VLSI DESIGN LAB

**L – T – P**
**0 - 0 - 3**

**List Of Experiments.**

1. Design CMOS Inverter.
2. Design CMOS AND Gate.
3. Design CMOS OR Gate.
4. Design CMOS NAND Gate.
5. Design CMOS EX-OR Gate.
6. Design CMOS EX-NOR Gate
7. Design SR NAND Latch.
8. Design SR NOR Latch.
9. Design CMOS Invert Layout.
10. Design CMOS NOR Gate.

## MT-VLES -513 EMBEDDED SYSTEM DESIGN LAB

**L – T – P**
**0 - 0 - 3**

1. Design With S bit Microcontrollers 8051 pic micro controllers- Assembly and C Programming: IO Programming. Timers.
2. Interrupts. Serial port programming with 8051 pic microcontrollers. Assembly and C Programming.
3. PWM Generation Motor Control. ADC DAC with 8051 pic Microcontrollers-Assembly and C programming.
4. LCD and RTC interfacing .Sensor Interfacing 8051 PIC Microcontrollers-Assembly and C Programming.
5. Design with 16-bit Processors: L'O programming, Timers, Interrupts, Serial Communication.
6. Design with ARM Processors: I\O Programming ,ADC DAC,Timers, Interrupts.
7. Study of one type of real time Operating system(RTOS).
8. Simple wired wireless network simulation using NS2 Software.
9. Programming of TCP IP protocol stack.

# SECOND SEMESTER

## MT-VLES -502 ANALOG IC DESIGN

**L –T - P**
**4 – 0 - 0**

**Maximum marks:**100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Basic MOS Device Physics:** MOS IV Characteristics, Second order effects, Short-Channel Effects, MOS Device Models, Review of Small Signal MOS Transistor Models, MOSFET Noise.

**Analog MOS Process:** Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to Analog IC fabrication, Fabrication of active devices, passive devices and interconnects, Analog Layout Techniques, Symmetry, Multi-finger transistors, Passive devices: Capacitors and Resistors, Substrate Coupling, Ground Bounce.

**Single Stage Amplifiers:** Common Source Stage, Source Follower, Common Gate Stage, Cascade, Folded Cascade.

**Differential Amplifier:** Single ended and Differential Operation, Qualitative and Quantitative Analysis of Differential pair, Common Mode response, Gilbert Cell.

**Current Sources and Mirrors:** Current Sources, Basic Current Mirrors, Cascade Current Mirrors, Wilson Current Mirror, Large Signal and Small-Signal analysis.

**Frequency Response of Amplifiers:** Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.

**Voltage References:** Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References.

**Feedback:** General Considerations, Topologies, Effect of Loading.

**Operational Amplifier:** General Considerations, Theory and Design, Performance Parameters, Single-Stage Op Amps, Two-Stage Op Amps, Design of 2-stage MOS Operational Amplifier, Gain Boosting, Comparison of various topologies, slew rate, Offset effects, PSRR.

**Stability and Frequency Compensation:** General Considerations, Multi-pole systems, Phase Margin, Frequency Compensation, Compensation Techniques.

**Noise:** Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure.

**Switched-Capacitor Circuits:** Sampling Switches, Speed Considerations, Precision Considerations, Charge Injection Cancellation, Switched-Capacitor Amplifiers, Switched- Capacitor Integrator, Switched-Capacitor Common-Mode Feedback.

**Non Linearity and Mismatch:** Nonlinearity of Differential Circuits, Effect of Negative Feedback, Capacitor Nonlinearity, Linearization Techniques, Offset Cancellation Techniques, Reduction of Noise by Offset Cancellation.

**Reference Books**


1. Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill (2008).
2. Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley (2004).
3. Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002) 2nd ed.
4. Johns, D.A. and Martin, K., Analog Integrated Circuit Design, John Wiley (2008).
5. Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley (2001) 5th ed.

## MT-VLES -504 Embedded System Design-II

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**THE PIC MICROCONTROLLER ARCHITECTURE** :CPU, ALU , Data Movement, The Program Counter and Stack, Reset , Interrupts, Architecture Differences, Mid-Range instruction Set

**PIC HARDWARE FEATURES :**Power Input and Decoupling , Reset, Watchdog Timer, System Clock/Oscillators, Configuration Registers, Sleep , Hardware and File Registers, Parallel Input Output, Interrupts, Prescaler , The OPTION Register , Mid-Range Built-In EEPROM Flash Access, TMR1 andTMR2 Serial I/0, Analog I/0, Parallel Slave Port (PSP), External Memory Connections , In-Circuit Serial Programming (ISCP).

**PROGRAMMING WITH PIC :**Assembly Language Programming, Hex File Format, Code-Protect Features, Programming, PIC Emulators .

**HARDWARE LNTERFACING :**Estimating Application Power Requirements, Reset, lnterfacing to External Devices, LEDs, Switch Bounce , Matrix Keypads , LCDs, Analog I/O, Relays and Solenoids, DC and Stepper Motors, Servo Control Serial Interfaces .

**ARM PROCESSOR FUNDAMENTALS :**Registers, State and Instruction Sets, Pipeline, Memory Management, Introduction to the ARM Instruction Set

**Reference books:**


1. Programming and customizing PIC microcontroller- Myke Predko, Mc- Graw Hill.
2. John.B. Peatman, “Design with PIC Micro controller”, Pearson Education, 2003.
3. Steave Furber, “ARM system – on – chip architecture” Addison Wesley, 2000.

## MT-VLES -506 Low Power VLSI Design

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Low power Basics:** Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

**Device & Technology Impact on Low Power:** Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

**Power estimation Simulation Power analysis:** SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. .

**Low Power Design Circuit level:** Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

**Logic level:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

**Low power Architecture & Systems:** Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

**Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network

**Algorithm & architectural level methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

**Reference Books:**

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002

2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997
3. Kaushik Roy, Sharat Prasad,“Low-Power CMOS VLSI Circuit Design” Wiley,2000

## MT-VLES -508 Embedded System for Wireless & Mobile Communication

**L –T - P**
**4 – 0 - 0**

**Maximum marks:**100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol

Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping

Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatter net

Connection establishment procedure, notable aspects of connection establishment, Mode of connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile, Secondary bluetooth profile

Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers

Programming with Java: Java Programming, J2ME architecture, Javax. bluetooth package Interface, classes, exceptions, Javax. obex Package: interfaces, classes

Bluetooth services registration and search application, bluetooth client and server application. Overview of IrDA, HomeRF, Wireless LANs, JINI

**Reference books:**


1. Bluetooth Technology by C.S.R. Prabhu and A.P. Reddi; PHI
2. Wireless communication by Rappaport
3. Mobile communication by Schiller
4. Mobile communication by C.Y.Lee

# MT-VLES -510 Embedded System Design – II LAB

**L – T – P**
**0 - 0 - 3**

**1. Decimal Counter and Multiplexing the Output**

The purpose of this lab is to implement a decimal counter, which counts from 0 to 99. The students will be required to write a program for the AVR 8515 micro-controller.

**2. Watchdog Timer**

In this lab the students will design a hardware watchdog timer. They are ment to write a buggy program in order to test their WDT. The 8515 program should perform some computation, e.g., write 1, 2, 3 ... to the LED and at some point enter an infinite loop. During normal operation, the 8515 program must periodically (up to 254 second long cycles) write to the WDT's initial value register to avoid unnecessary resets.

**3. AVR microcontroller UART in C**

Implement AVR microcontroller UART in C

**4. Implementation of simple calculator using AVR 8515**

Implement a simple calculator using AVR 8515 microcontroller with keyboard and LCD display interface.

**5. Analog to Digital Conversion**

To be able to implement analog to digital conversion using the ADC0804LCN 8-bit A/D converter. You will design a circuit and program the chip so that when an analog signal is given as input, the equivalent digital voltage is displayed on an LCD display.

**6. Implementing SPI bus Using AVR 8515**

The students are required to implement I2C serial communication using AVR 8515.

**7. Digital Filters with AVR**

Implement digital filters using low cost microcontroller from AVR series.

**8. Converting 8-bit LCD communication to 4-bit**

Interface LCD with AVR 8515 using only 4 microcontroller pins

**9. IR Remote Control Receiver**

In this lab students are required to design and implement IR remote control receiver using AVR 8515 microcontroller

10. **Step Motor Controller** In this lab students are meant to implement a compact size and high-speed interrupt driven step motor controller.

**11.A Temperature Monitoring and Acquisition** System with LCD Output and memory interface

Implement this using the SDK- 500 Kit for AVR.

## MT-VLES -512 ANALOG IC DESIGN LAB

**L – T – P**
**0 - 0 - 3**

**List of Experiments.**

1. Common Source Amplifier
2. Cascade Amplifier
3. Push Pull Amplifier
4. Folded Cascade Amplifier .
5. Current Mirror.
6. Cascaded Current Mirror.
7. Differential Amplifier
8. CMOS Op-amp single Stage.
9. Common Drain Amplifier .
10. Common Gate Amplifier.
11. Current Controlled Voltage source.

# THIRD SEMESTER

**MT-VLES -601 Adaptive Signal Processing**

**L –T - P**
**4 – 0 - 0**

**Maximum marks:**100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Basic Of Digital Signal Processing:** Signals and Information, Signal Processing Methods, Applications of Digital Signal Processing, Derivation of the z-Transform Properties of z-Transform, Fourier series and Fourier transform., Random variable, Stochastic processes.

**Design Of Digital Filters:** Introduction, Linear Time-Invariant Digital Filters, Recursive and Non-Recursive Filters, Filtering Operation, Sum of Vector Products, A Comparison of Convolution and Correlation, Filter Structures, Direct, Cascade and Parallel Forms, Linear Phase FIR Filters Design of Digital FIR Filter-banks, Sub-band Filters, Design of Infinite Impulse Response IIR filters, Issues in the Design and Implementation of a Digital Filter.

**Estimation Theory**: Bayesian Estimation Theory, Basic Definitions, Bayesian Estimation, Expectation Maximization Method, Generalized Parameter Estimation, Cramer–Rao lower Bound on the variance of estimator, maximum likelihood estimation, Design of Gaussian Mixture Models , Bayesian Classification, Modeling the Space of a Random Process, Detection

**AdaptiveFiltering:** State-Space Kalman Filters, Recursive Least Square (RLS) Adaptive Filters The Steepest-Descent Method LMS Filter, Different Algorithms and their Variants used in adaptive filtering and their performance criteria. Multirate Signal Processing

**Applications:** Applications of adaptive Digital Signal Processing to Speech, Music and Telecommunications, Parameter estimation, System identification, Noise and Echo cancellation, Acoustic source localization techniques, Channel Equalization.

BOOKS:

1. Siomon S Haykins, “Adaptive Filter Theory,”PHI, 3rd Edition
2. Proakis,”Digital Signal Processing,”PHI 2nd edition
3. Harry L. Van Trees, “ Detection, Estimation, and Modulation Theory, Part 1&3,” Wiley 2002
4.Saeed V. Vaseghi, “Advanced Digital Signal Processing and Noise Reduction,” Third Edition,2006
5. Eberhard Hänsler, “Gerhard Schmidt Acoustic Echo and Noise Control: A Practical Approach,”wiley,2005

## MT-VLES -603 Embedded Control System

**L –T - P**
**4 – 0 - 0**

**Maximum marks:**100 **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**INTRODUCTION** Controlling the hardware with software – Data lines, Address lines, Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

**INPUT-OUTPUT DEVICES** Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules, LCD module display, Configuration – Time-of-day clock –Timer manager – Interrupts – Interrupt service routines, IRQ, ISR, Interrupt vector or dispatch table multiple-point – Interrupt-driven pulse width modulation.

**D/A AND A/D CONVERSION** R 2R ladder – Resistor network analysis – Port offsets – Triangle waves analog vs. digital values – ADC0809 – Auto port detect – Recording and playing back voice – Capturing analog information in the timer interrupt service routine – Automatic, multiple channel analog to digital data acquisition.

**ASYNCHRONOUS SERIAL COMMUNICATION** Asynchronous serial communication – RS-232, RS-485 – Sending and receiving data –Serial ports on PC – Low-level PC serial I/O module, Buffered serial I/O.

**CASE STUDIES: EMBEDDED C PROGRAMMING** Multiple closure problems – Basic outputs with PPI – Controlling motors – Bi-directional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

**REFERENCE BOOKS:**

1. Jean J. Labrosse, “Embedded Systems Building Blocks: Complete and Ready-To-Use Modules in C”, The publisher, Paul Temme, 2003.
2. Ball S.R., „Embedded microprocessor Systems – Real World Design□, Prentice Hall, 2001.
3.. Herma K, “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 2003.
4.. Daniel W. Lewis, “Fundamentals of Embedded Software where C and Assembly meet”, PHI, 2002.

**MT-VLES -605 Adaptive Signal Processing Lab**

**L – T – P**
**0 - 0 - 3**

List of Experiments:
1. Write matlab statement for algebraic equations.
2. Designing Filters from Windowing techniques.
3. Write matlab programme to find the Power spectral Density.
4. Matlab Programme for Ploting different Graphs.
5. Filter design with the help of matlab filter design tool.
6. Simulation of the given model using Simulink tool.
7 Matlab programme for cross correlation and auto correlation .
8. Working with DSP Processor &Hardware.

## MT-VLES -607 SEMINAR

Every student will be required to present a seminar talk on a topic approved by the Deptt. . The committee constituted by the Head of the Deptt. Will evaluate the presentation and will award the marks.

## MT-VLES -609 Minor Project

Identification of faculty supervisor(s), topic, objectives, deliverables and work plan (in the preceding semester); regular work during semester with weekly coordination meetings of about 1 hour duration with the faculty supervisor, and an end-semester demonstration to Project Evaluation Committee. Marks to be decided on the basis of a mid-term and an end-semester presentation following the demonstration vis-vis the approved work plan. The topic should be of advanced standing requiring use of knowledge from program core courses and be preferably hardware oriented. Topic will have to be different from the major project.

## FOURTH SEMESTER

## MT-VLES -602 DISSERTATION

The Dissertation Phase-1 will be continued as dissertation in 4th Semester. The award of sessional grades out of A+, A, B, C, D and E will be done by an internal Committee constituted by the Head of the Deptt. This assessment shall be based on presentation (s), report, etc. before this committee. In case a student scores 'F' –grade in the sessional, failing which he/ she will not be allowed to submit the dissertation. At the end of the semester, every student will be required to submit three bound copies of his/her Master's dissertation of the office of the concerned Department. Out of these, one copy will be kept for department record & one copy shall be for the supervisor. A copy of the dissertation will be sent to the external examiner by mail by the concerned department, after his/her appointment and intimation from the university. Dissertation will be evaluated by a committee of examiners consisting of the Head of the Department, dissertation supervisor(s) and one external examiner. There shall be no requirement of a separate evaluation report on the Master Dissertation from the external examiner. The external examiner shall be appointed by the University from a panel of examiners submitted by the respective Head of Deptt., to the Chairman, Board of Studies. In case the external examiner so appointed by the University does not turn up, the Director/ Principal of the concerned college, on the recommendation of the concerned Head of the Deptt. Shall be authorized, on behalf of the University., to appointed an external examiner from some other institution. The student will defend his/her dissertation through presentation before this committee and the committee will award one of the grades out of A+, A, B, C, D and E Student scoring 'F' grade in the exam shall have to resubmit his/her Dissertation after making all correction / improvements and this dissertation shall be evaluated as above.

**ELECTIVE – 1**

## MT-VLES -514 NanoTechnology

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Atomic structure**
Basic crystallography, Crystals and their imperfections, Diffusion, Nucleation and crystallization, Metals, Semiconductors and Insulators, Phase transformations , Ceramic materials.

**Physical Properties of Materials**
Electrical and Thermal properties, Optical properties of materials, Magnetic properties of materials, Density of states, Coulomb blockade, Kondo effect,Hall effect,Quantum Hall Effect.

**Nanostructures**
Introduction to Nanotechnology, Zero dimensional nanostructures - Nano particles, One dimensional nanostructures - Nano wires and Nano rods, Two dimensional nanostructures - Films, Special nano materials, Nano stuctures fabricated by Physical Techniques, Properties of Nanomaterials, Applications of Nano structures, Basics of Nano Electronics.

**Characterization of Nanomaterials**
SPM Techniques - Scanning Tunneling Microscopy, Atomic Force Microscopy, Magnetic Force Microscopy, Electron Microscopy - Scanning Electron Microscope, Transmission Electron Microscope

**Reference Books ;**

1.Introduction to solid state Physics: C.Kittel
2. Introduction to theory of solids: H.M. Roenberg
3. Physics and Chemistry of materials: Joel I. Gersten
4.Handbook of Nanotechnology: Bharat Bhushan(springer)

**ELECTIVE - 1**

## MT-VLES -516 Mixed Signal Embedded System

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**INTRODUCTION TO SYSTEM DESIGN**

Dynamic Range, Calibration, Bandwidth, Processor Throughput, Avoiding Excess Speed , Other System Considerations, Sample Rate and Aliasing

**DAC & ADC Introduction**

converters - High speed ADC design, High speed DAC design and Mixed signal design for radar application - ADC and DAC modules used for LIGO.

**PLL**

Introduction - Frequency Synthesizers - Design of PLL and Frequency Synthesizers - PLL with voltage driven oscillator- PLL with current driven oscillator- ETPLL - PLL synthesizer oscillator by MC14046B

**SENSOR INTERFACING**

Sensors, Sensor Types, Amplifier Design, Interfacing of Temperature, Pressure, Displacement Transducer in Embedded System Environment

**LCD AND INFRA RED**

LCD Fundamentals, Response Time, Temperature Effects, Connection Methods, Different types of LCD Panels, Static Waveforms, Infra Red Detection and Transmission

**TIME-BASED MEASUREMENTS**

Measuring Period versus Frequency , Mixing, Voltage-to-Frequency Converters, Clock Resolution and Range, Extending Accuracy with Limited Resolution

**REFERENCE BOOKS:**

1. Analog Interfacing to Embedded Microprocessors Real World Design, Stuart Ball.
2. Breems, “Continuous-Time Sigma Delta Modulations for A/D Conversion”,. Kluwer, 2002.
3. Allen, “CMOS Analog Circuit Design”, Oxford, 2005.
4. Behzad Razavi, “Design of Analog CMOS integrated circuit”, Tata McGraw Hill,

**ELECTIVE - 1**

**L –T - P**
**4 – 0 - 0**

## MT-VLES -518 VLSI Testing and Design for Testability

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Physical defects and their modeling;** stuck at faults; Bridging Faults; Fault collapsing. Fault Simulation: Deductive, Parallel and Concurrent; Critical Path Tracing.

**Test Generation for Combinational Circuits:** D-Algorithm, Boolean Difference, PODEM, and ATPG.

**Random, Exhaustive and Weighted**: Random Test Pattern Generations Aliasing and its effect on Fault coverage.

**PLA Testing**: cross-point Fault Model, Test Generation,

**Memory testing**: Permanent Intermittent and Pattern Sensitive Faults; Delay Faults and Hazards; Test Generation Techniques;

**Test Generation for Sequential Circuits.**

**Scan Design. Scan path and LSSD, BILBO**

**Concept of Redundancy, spatial redundancy, Time redundancy**

**Recent trends in VLSI testing:** Genetic Algorithms, Parallel Algorithms, Neural networks, nano scale testing

**Reference books:**

1. VLSI Testing: digital and mixed analogue digital techniques Stanley L. Hurst Pub:Inspec/IEE ,1999

2. VLSI Test Principles and Architectures: Design for Testability By: Laung-Terng Wang; Cheng-Wen Wu; Xiaoqing Wen

3. Advanced Simulation and Test Methodologies for Vlsi Design by Gordon Russell

4. Vlsi Testing: Digital and Mixed Analogue/Digital Techniques by Stanley Leonard Hurst

**ELECTIVE - II**

**MT-VLES -611 NEURAL NETWORKS & FUZZY LOGIC**

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Introduction:** Neural networks characteristics, History of development in neural networks principles, Artificial neural net terminology, Model of a neuron, Topology.

**Learning Methods & Neural network models**: types of learning, Supervised, Unsupervised, Re-enforcement learning. Knowledge, representation and acquisition. Basic Hop field model, Basic learning laws, Unsupervised learning, Competitive learning, K-means clustering algorithm, Kohonen's feature maps.

**Artificial Neural Networks:** Radial basis function neural networks, Basic learning laws in RBF nets, Recurrent back propagation. Introduction to counter propagation networks, CMAC network, and ART networks.

**Applications of neural nets:** Applications such as pattern recognition, Pattern mapping, Associative memories, speech and decision-making..

**Fuzzy Logic:** Basic concepts of fuzzy logic, Fuzzy vs. Crisp set, Linguistic variables, Membership functions, Fuzzy sets & Operations of fuzzy sets, Fuzzy IF- THEN rules, Variable inference techniques, De-Fuzzification, Basic fuzzy inference algorithm, Fuzzy system design, Antilock Breaking system (ABS), Industrial applications.

**Reference Books:**


1. B. Yegnanarayana, " Artificial Neural Networks"PHI
2. J.M. Zurada, "Introduction to artificial neural systems", Jaico Pub.
3. ROSS J.T , "Fuzzy logic with engineering application", TMH
4. Simon Haykin, "Neural Networks", PHI
5. Ahmad M.Ibrahim, "Introduction to applied Fuzzy Electronics", (PHI)
6. P.D. wasserman , "Neural computing theory & practice", (ANZA PUB).

**ELECTIVE - II**

## MT-VLES -613 Cryptology and Crypto chip Design

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Basic concepts :** Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS,, Targets: Hardware, Software, Data communication procedures. Threats to Security: Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security.

**Encryptions Techniques:** Conventionnel techniques, Modern techniques, DES, DES chaining+, Triple DES, RSA algorithme, Key management. Message Authentication and Hash Algorithm: Authentication requirements and functions secure Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service.

**Firewalls and Cyber laws:** Firewalls, Design Principles, Trusted systems, IT act and cyber laws, Virtual private network. Future Threats to Network: Recent attacks on networks, Case study

**Applications:** AES algorithme. Crypto chip design: Implementation of DES, IDEA AES algorithm, Development of digital signature chip using RSA algorithm.

**Reference Books:**

1. William Stalling “Cryptography and Network Security” Pearson Education, 2005
2.Charels P. Pfleeger “Security in Computing” Prentice Hall, 2006

3.Jeff Crume “Inside Internet Security” Addison Wesley, 2000.

**ELECTIVE - II**

## MT-VLES -615 Computer Aided VLSI Design

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Hardware description languages;** Verifying behavior prior to system construction simulation and logic verification; Logic Synthesis PLA based synthesis and multilevel logic synthesis.

**Logic optimization;** Logic Simulation Compiled and event simulators; Relative advantages and disadvantages; Layout Algorithms Circuit partitioning, placement, and routing algorithms.

**Design rule verification;** Circuit Compaction; Circuit extraction and post-layout simulation; Automatic Test Program Generation.

**Combinational testing D-Algorithm and PODEM algorithm;** Scan-based testing of sequential circuits; Testability measures for circuits.

**Reference Books:**

1.“Algorithm and Data Structures for VLSI Design”, Christophn Meinel & Throsten Theobold, 2002.
2.“Evolutionary Algorithm for VLSI”, Rolf Drechsheler ,

**ELECTIVE - II**

## MT-VLES -617 Digital Image Processing

**L –T - P**
**4 – 0 - 0**

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**Introduction And Digital Image Fundamentals :**The origins of Digital Image Processing, Examples of Fields that Use Digital Image Processing, Fundamentals Steps in Image Processing, Elements of Digital Image Processing Systems, Image Sampling and Quantization, Some basic relationships like Neighbors, Connectivity, Distance Measures between pixels, Linear and Non Linear Operations.

**Image Enhancement in the Spatial Domain :**Some basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic and Logic operations, Basics of Spatial Filters, Smoothening and Sharpening Spatial Filters, Combining Spatial Enhancement Methods. Image Enhancement in the Frequency Domain. Introduction to Fourier Transform and the frequency Domain, Smoothing and Sharpening Frequency Domain Filters, Homomorphic Filtering. Image Restoration.

**A model of The Image Degradation** : Restoration Process, Noise Models, Restoration in the presence of Noise Only Spatial Filtering, Periodic Noise Reduction by Frequency Domain Filtering, Linear Position-Invariant Degradations, Estimation of Degradation Function, Inverse filtering, Wiener filtering, Constrained Least Square Filtering, Geometric Mean Filter, Geometric Transformations.

**Compression :** Image Compression Coding, Interpixel and Psycho visual Redundancy, Image Compression models, Elements of Information Theory, Error free comparison, Lossy compression, Image compression standards. Image Segmentation : Detection of Discontinuities, Edge linking and boundary detection, Thresholding, Region Oriented Segmentation, Motion based segmentation. Representation and Description :Representation, Boundary Descriptors, Regional Descriptors, Use of Principal Components for Description, Introduction to Morphology, Some basic Morphological Algorithms. Patterns and Pattern Classes, Decision-Theoretic Methods, Structural Methods

**Reference Books:**


1. Rafael C. Conzalez & Richard E. Woods, “Digital Image Processing”, 2nd edition, Pearson Education, 2004.
2. A.K. Jain, “Fundamental of Digital Image Processing”, PHI, 2003.
3. Rosefield Kak, “Digital Picture Processing”, 1999.
4. W.K. Pratt, “Digital Image Processing”, 2000.

**ELECTIVE - II**

**L –T - P**
**4 – 0 - 0**

## MT-VLES -619 Algorithms for VLSI Design Automation

**Maximum marks:** 150 (**External:** 100, **Internal:** 50) **Time:** 3 hrs

**Note :** In the Semester Examinations the examiner will set 8 questions in all, covering the entire syllabus and the student will be required to attempt only 5 questions. Each Question carry equal marks

**VLSI physical design automation and Fabrication** VLSI Design cycle, New trends in VLSI design, Physical design cycle, Design style, Introduction to fabrication process, design rules, layout of basic devices

**VLSI automation Algorithms Partitioning:** Problem formulation, classification of partitioning algorithms, Group migration algorithms, simulated annealing.

**Floor planning & pin assignment:** Problem formulation, classification of floor planning algorithms, constraint based floor planning, floor planning algorithms for mixed block & cell design, chip planning, pin assignment, problem formulation, classification of pin assignment algorithms, General & channel pin assignment Placement Problem formulation, classification of placement algorithms, simulation base placement algorithms, recent trends in placement

**Global Routing and Detailed routing:** Problem formulation, classification of global routing algorithms, Maze routing algorithm, line probe algorithm, Steiner Tree based algorithms, performance driven routing Detailed routing problem formulation, classification of routing algorithms, introduction to single layer routing algorithms, two layer channel routing algorithms, greedy channel routing, switchbox routing algorithms.

**Over the cell routing & via minimization:** Two layers over the cell routers, constrained & unconstrained via minimization

**Compaction:** Problem formulation, classification of compaction algorithms, one-dimensional compaction, two dimension based compaction, hierarchical compaction

**Reference Books :**


1. Naveed Shervani, “Algorithms for VLSI physical design Automation”, Kluwer Academic Publisher, Second edition.
2. Christophn Meinel & Thorsten Theobold, “Algorithm and Data Structures for VLSI Design”, KAP, 2002.
3. Rolf Drechsheler : “Evolutionary Algorithm for VLSI”, Second edition