UNIVERSITY INSTITUTE OF ENGINEERING & TECHNOLOGY MAHARSHI DAYANAND UNIVERSITY, ROHTAK SCHEME OF STUDIES & EXAMINATIONS

Doctor of Philosophy (Ph.D.) – Electronics and Communication Engg.
Jan,17 to Dec,17

i) The duration of the Ph.D. course will be of one semester.
ii) The Department concerned shall design the Ph.D. course as per latest guide lines of UGC which are:

"The Ph.D. course must include a course on research methodology which may include quantitative methods and computer applications. It may also involve review of published research in relevant area".

iii) The scheme for Pre-Ph.D. course work is as under:
a) Common course:

17ECEPCC1: Research Methodology (Quantitative Techniques and Computer Applications in Research)

b) Departmental course:

17ECEPCC2: Review of Literature and Seminar (in Relevant Research Area)
Departmental – Elective Course (in Relevant Research Area)

iv) The qualifying marks in each paper of the course work shall be 50%.
vi) It is only on satisfactory completion of Ph.D Programme, which shall be an essential part and parcel of the Ph.D. programme that a candidate shall be eligible to apply for registration in Ph.D. Programme.

Sr. No.	Course No.	Course Title	Marks of	Examination Marks		Total Mark	Duration of Exam
				Theory	Practical		
1	17ECEPCC1	Research Methodology (Quantitative Techniques and Computer Applications in Research)	20	80	-	100	3
2	17ECEPCC2	Review of Literature and Seminar (in Relevant Research Area)	20	-	80	100	3
3		Departmental – Elective Course (in Relevant Research Area) any one from the list attached	20	80	-	100	3
	Total		60	160	80	300	

* Marks of internal assessment of theory courses are based two assignments of 10 marks each.

Program Specific Outcomes- Ph.D.(ECE)

At the end of the programme, the student shall be able to

PSO1: acquire the necessary theoretical tools as well practical tools to undertake the research in various fields of Electronics & Communication Engineering.

PSO2: Get expertise in understanding, formulating and solving new and cutting edge problems in various fields of Electronics & Communication Engineering.

PSO3 : Address the problems of society and industrial interests in various applicable themes.

PSO4 :Produce and disseminate the new knowledge in high quality, peer reviewed research journals and Ph.D. thesis.

PSO5: conduct scholarly or professional activities in an ethical manner.

List of Electives:

1	17ECEPCD1	Advanced Data Communications
2	17ECEPCD2	Advanced Digital Signal processing
3	17ECEPCD3	Coding Theory and Techniques
4	17ECEPCD4	CPLD & FPGA Architectures and Applications
5	17ECEPCD5	Device Modeling
6	17ECEPCD6	Digital Control Systems
7	17ECEPCD7	Digital System Design
8	17ECEPCD8	Embedded Real Time Operating Systems
9	17ECEPCD9	Internetworking
10	17ECEPCD10	Micro Electromechanical Systems
11	17ECEPCD11	Microcontrollers for Embedded system Design
12	17ECEPCD12	Network Security & Cryptography
13	17ECEPCD13	Neural Networks And Fuzzy Systems
14	17ECEPCD14	High Speed Networks
15	17ECEPCD15	Micro Processor And Microcontrollers
16	17ECEPCD16	Robotics
17	17ECEPCD17	Satellite Communications
18	17ECEPCD18	Telecommunication Switching & Networks
19	17ECEPCD19	VLSI Technology and Design
20	17ECEPCD20	Adhoc Wireless & Sensor Networks
21	17ECEPCD21	Algorithms for VLSI Design Automation
22	17ECEPCD22	CMOS Analog & Mixed Signal Design
23	17ECEPCD23	Design for Testability
24	17ECEPCD24	Detection and Estimation Theory
25	17ECEPCD25	Digital Signal Processors and Architectures
26	17ECEPCD26	Hardware Software Co-Design
27	17ECEPCD27	Image & Video Processing
28	17ECEPCD28	Mobile Computing Technologies
29	17ECEPCD29	Optical Communications Technology
30	17ECEPCD30	Optical Networks
31	17ECEPCD31	Propagation Models for Wireless Communications
32	17ECEPCD32	Radar Signal Processing
33	17ECEPCD33	RF Circuit Design
34	17ECEPCD34	Semiconductor Memory Design & Testing
35	17ECEPCD35	Speech Processing
36	17ECEPCD36	System Modeling and Simulation
37	17ECEPCD37	System On Chip Architecture
38	17ECEPCD38	VLSI Signal Processing
39	17ECEPCD39	Voice over Internet Protocol
40	17ECEPCD40	Wireless Communications & Networks
41	17ECEPCD41	Transform Techniques
42	17ECEPCD42	EMI/EMC
43	17ECEPCD43	Microwave Circuits & Microwave Integrated Circuits
44	17ECEPCD44	Global Positioning Systems
45	17ECEPCD45	Microwave Antennas

Note: The departmental elective subjects will be offered as per availability of expertise and the required infrastructure in the department.

RESEARCH METHODOLOGY
(Quantitative Techniques and Computer Applications in Research)

Subject Code: 17ECEPCC1

Course Outcomes:

By the end of the course the students will be able to:

CO1 Learn the concept of research, research process, types of research, research models and basics formats of report writing.
CO2 Learn the use of statistical analytic techniques for data analysis and testing of hypothesis.
CO3 Identify the differences between measurement and scaling and how sample is selected and determined using various approaches.
CO4 To understand sources of data collection and how data is collected from different sources.
CO5 To understand the concept of interpretation and role of computer in mathematical and Statistical analysis with applications of relevant research methodologies used in electronic science & Engineering.

17ECEPCC1: Research Methodology
(Quantitative Techniques and Computer Applications in Research)

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D	Marks of Internal:	20
3	-	-	Examination:	80
Duration of Exam: 3 Hrs			Total Marks:	100

UNIT I Element of Research

Scientific process meaning and definition, a brief history of scientific process. Introduction to research methodology- Meaning of research, objective of research, types of research, significance of research, problem encountered by researchers in india, Research problem- Definition, necessity and techniques of defining research problem, formulation of research problem, objective of research problem, research design- Meaning, need and features of good research design, types of research designs, basic principles of Experimental design.

UNIT II Sampling Hypothesis & Statistical Analysis

Sampling design, census and sample surveys, different types of sample designs, characteristics of good sample design, Techniques of selecting a random sample. Data collection-primary and secondary data, methods of selecting primary and secondary data, hypothesis- definition, testing of hypothesis, procedures of hypothesis testing, flow

diagram for hypothesis testing, parametric and non-parametric tests for testing of hypothesis, limitations of tests of hypothesis.

Hypothesis tests- One sample test-two sample tests/ chi square tests, association of attributes. T-tests, statical analysis, correlation and regression analysis- analysis of variance, completely randomized design, randomized complete block design, Latin square design-partial and multiple correlations – discriminent analysis - cluster analysis – principle component and factor analysis, repeated measure analysis. Probability and probability distributions; Binomial, Poisson, distribution, Basic ideas of testing of hypotheses; Tests of significance based on normal distributions.

UNIT III Paper Writing and Report Generation

Basic concepts of paper writing and report generation, review of literature, concepts of bibliography and references, significance of report writing, steps of report writing, types of research reports, methods of presentation of report.

UNIT IV Computer Applications in Research

Computer Applications: Fundamentals of computers-Definition, types of computers, RAM, ROM, CPU, I/O devices, Number systems-Binary, octal and hexadecimal, base conversion, logic gates- AND, OR, NOT, Data structure array, stack (push, pop), queue (insert, delete), linked list-singly, doubly, operating system-definition, types of operating system, uses of software's MS-Office-Power point, word, Excel and Access.

Text Books:

1. C. R. Kothari – Research Methodology Methods and Techniques – Wishwa Prakashan Publishers – Second Edition.

17ECEPCC2: Review of Literature and Seminar (in Relevant Research Area)

Course Outcomes (COs): After studying this course, students will be able:
CO 1- understand basic elements of research and write a relevant paper after reviewing literature
CO 2- Understand hypothesis and statistical analysis
CO 3- Knowledge of writing research paper
CO 4- present/communicate a research paper in a conference/journal.

1. The research student is required to prepare a concept paper/working, paper/review paper by reviewing at least 50 research papers / references books / unpublished doctoral dissertations / other reports etc.

2. To qualify the paper the research student is required either to present the prepared paper in a International Conference/ Seminar/ Workshop or published the same in a research journal. Acceptance for publication or presentation will be considered as published/ presented.

3. A duly constituted committee of three teachers of the department by the Director/Head shall evaluate the completion of the paper.

ADVANCED DATA COMMUNICATION

Subject Code: 17ECEPCD1

Course Outcomes:

By the end of the course the students will be able to:

CO1. To create understanding of different digital modulation techniques and able to differentiate between different techniques on the basis of bandwidth efficiency, carrier recovery.

CO2. To learn various basic concepts related to data communication and gain knowledge of various interfaces used in communication.

CO3. To understand difference between various error correction and detection techniques and gain knowledge of various synchronous and asynchronous data link protocols.

CO4. To learn basic difference between various multiplexing techniques and get to learn various multiple access techniques.

17ECEPCD1: Advanced Data Communication

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	**-**	**-**	**Examination:**	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit-I:

Digital Modulation: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

Unit -II:

Basic Concepts of Data Communications, Interfaces and Modems: Data Communication- Components, Networks, Distributed Processing, Network Criteria- Applications, Protocols and Standards, Standards Organizations- Regulatory Agencies, Line Configuration- Point-to-point- Multipoint, Topology- Mesh- Star- Tree- Bus- Ring- Hybrid Topologies, Transmission Modes- Simplex- Half duplex- Full Duplex, Categories of Networks- LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE- DCE Interface- Data Terminal Equipment, Data Circuit- Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

Unit-III:

Error Detection and Correction: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check)- Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code.

Data link Control: Stop and Wait, Sliding Window Protocols.

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols – HDLC, Link Access Protocols.

Unit-IV:

Switching: Circuit Switching- Space Division Switches- Time Division Switches- TDM Bus- Space and Time Division Switching Combinations- Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach- Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.
Multiplexing: Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.
Multiple Access: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization- Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 3rd ed., 2008, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5 ed., 2008, PEI.

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.
3. Data Communication and Tele Processing Systems - T. Housely, 2nd Edition, 2008, BSP.
4. Data Communications and Computer Networks- Brijendra Singh, 2nd ed., 2005, PHI.
5. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

ADVANCED DIGITAL SIGNAL PROCESSING

Subject Code: 17ECEPCD2

Course Outcomes:

By the end of the course the students will be able to:

CO1. To create understanding of discrete transforms and basic techniques of filters.

CO2. To gain knowledge of various parameters related to multi rate signal processing.

CO3. To acquire a thorough knowledge of different power spectrum estimation as well as forward and backward linear estimation methods.

17ECEPCD2: ADVANCED DIGITAL SIGNAL PROCESSING

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT I

Review of DFT, FFT, IIR Filters, FIR Filters,

Multirate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing

UNIT II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Non-Parametric methods

UNIT III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & Its Properties, Relation between auto correlation & model parameters, AR Models - Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT –IV

Linear Prediction : Forward and Backward Linear Prediction – Forward Linear Prediction, Backward Linear Prediction, Optimum reflection coefficients for the Lattice Forward and Backward Predictors. Solution of the Normal Equations: Levinson Durbin Algorithm, Schur Algorithm. Properties of Linear Prediction Filters

Finite Word Length Effects: Analysis of finite word length effects in Fixed-point DSP systems – Fixed, Floating Point Arithmetic

TEXTBOOKS:

1. Digital Signal Processing: Principles, Algorithms & Applications - J.G.Proakis & D.G.Manolokis, 4th ed., PHI.
2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.
3. DSP – A Pratical Approach – Emmanuel C.Ifeacher, Barrie. W. Jervis, 2 ed., Pearson Education.

REFERENCES:

1. Modern spectral Estimation : Theory & Application – S. M .Kay, 1988, PHI.
2. Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education
3. Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000,TMH

Coding Theory and Techniques

Subject Code: 17ECEPCD3

Course Outcomes:

By the end of the course the students will be able to:

CO1. To understand various types of errors and various codes used for error correction and error detection.

CO2. Gain ability to differentiate between different linear and non-linear codes.

CO3. Knowledge related to merits and demerits of various codes is also acquired.
CO4. To implement error correction and detection.

17ECEPCD3: Coding Theory and Techniques

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:	3 Hrs			Total Marks:	100

UNIT-1

Coding for Reliable Digital Transmission and storage:
Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.
Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT-II

Cyclic codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT-III

Convolutional codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT-IV

Burst –Error-Correcting codes:
Decoding of Signle-Burst error Correcting Cyclic codes, Single-Burst-Error-Correcting Cyclic codes, Burst-Error-Correcting Convoulutional Codes, Bounds on Burst Error-Correcting

Capability, Interleaved Cyclic and Convolutional Codes , Phased-Burst –Error-Correcting Cyclic and Convolutional codes.

BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes- Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction

TEXT BOOKS:

1 Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J.Costello,Jr, Prentice Hall, Inc.

2 Error Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill Publishing.

REFERENCES:

1. Digital Communications-Fundamental and Application - Bernard Sklar, PE.

2. Digital Communications- John G. Proakis, 5th ed., 2008, TMH.

3. Introduction to Error Control Codes-Salvatore Gravano-oxford

4. Error Correction Coding – Mathematical Methods and Algorithms – Todd K.Moon, 2006, Wiley India.

5. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Edition, 2009, TMH.

CPLD & FPGA Architectures and Applications

Subject Code: 17ECEPCD4

Course Outcomes:

By the end of the course the students will be able to:

CO1. Compare different types of programmable logic devices.

CO2. Implement FPGA and evaluate its speed performance.
CO3. To understand hardware utilization for memory mapping.
CO4. To able to learn optimum utilization of memory and storage methodology.

17ECEPCD4: CPLD & FPGA Architectures and Applications

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT –I

Programmable logic : ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1to 5), Cypres FLASH 370 Device technology, Lattice PLST's architectures – 3000 series – Speed performance and in system programmability.

UNIT – II

FPGAs: Field Programmable gate arrays- Logic blocks, routing architecture, design flow technology mapping jfor FPGAs, Case studies Xitir x XC4000 & ALTERA's FLEX 8000/10000
FPGAs: AT &T ORCA's (Optimized Reconfigurable Cell Array): ACTEL's ACT-1,2,3 and their speed performance

UNIT-III

Alternative realization for state machine chat suing microprogramming linked state machine one –hot state machine, petrinetes for state machines-basic concepts, properties, extended petrinetes for parallel controllers.

UNIT-IV

Digital front end digital design tools for FPGAs& ASICs: Using mentor graphics EDA tool ("FPGA Advantage") – Design flow using FPGAs
Case studies of paraller adder cell paraller adder sequential circuits, counters, multiplexers, parellel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994,
Kluwer Academic Publications.
2. Field Programmable Gate Arrays, John V.Oldfield, Richard C Dore, Wiley Publications.

REFERENCES:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad,
1994, Prentice Hall.
2. Digital System Design using Programmable Logic Devices – Parag.K.Lala, 2003, BSP.
3. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier.

Device Modeling

Subject Code: 17ECEPCD5

Course Outcomes:

By the end of the course the students will be able to:

CO1. To create basic understanding of semiconductor physics .

CO2. To gain complete knowledge about VLSI fabrication design steps and implement modeling of hetero junction devices.

CO3. To understand integrated devices thoroughly.
CO4. To able to program a hardware for optimum functioning.

17ECEPCD5: Device Modeling

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:		3 Hrs		Total Marks:	100

UNIT I:

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, continuity equation, Poisson equation
Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, dependence of model parameters on structures

UNIT II:

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – static and dynamic behavior – small and large signal models – SPICE models
Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model- dynamic model, parasitic effects – SPICE model – parameter extraction

UNIT III:

Integrated MOS Transistor: nMOS and pMOS transistor – threshold voltage – threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT IV:

VLSI Fabrication Techniques: An overview of wafer fabrication, wafer processing – oxidation – patterning – diffusion – ion implantation – deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – interconnects circuit elements

Modeling of Hetero Junction Devices: Band gap Engineering, Bandgap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid state circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCES:

1. Physics of Semiconductor Devices – Sze S. M, 2nd edition, Mcgraw hill, New York, 1981
2 Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.

Digital Control Systems

Subject Code: 17ECEPCD6

Course Outcomes:

By the end of the course the students will be able to:

CO1. Establish comparison between digital to analog and analog to digital conversion.

CO2. To gain ability to perform stability analysis procedure.

CO3. To gain knowledge related to controllability and observability.
CO4. To able to design a optimum microcontroller device.

17ECEPCD6: Digital Control Systems

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT – I

SAMPLING AND RECONSTRUCTION: Introduction, Examples of Data control systems – Digital to Analog conversion and Analog to Digital conversion, sample and hold operations.
TRANSFORM ANALYSIS OF SAMPLED-DATA SYSTEMS: Introduction, Linear difference equations, pulse response, Z – transforms, Theorems of Z – Transforms, the inverse Z – transforms, Modified Z- Transforms
Z-PLANE ANALYSIS OF DISCRETE-TIME CONTROL SYSTEM: Z-Transform method for solving difference equations; Pulse transforms function, block diagram analysis of sampled – data systems, mapping between s-plane and z-plane.

UNIT – II

STATE SPACE ANALYSIS: State Space Representation of discrete time systems, Pulse Transfer Function Matrix solving discrete time state space equations, State transition matrix and it's Properties, Methods for Computation of State Transition Matrix, Discretization of continuous time state – space equations
CONTROLLABILITY AND OBSERVABILITY: Concepts of Controllability and Observability, Tests for controllability and Observability. Duality between Controllability and Observability, Controllability and Observability conditions for Pulse Transfer Function

UNIT – III

STABILITY ANALYSIS: Mapping between the S-Plane and the Z-Plane – Primary strips and Complementary Strips – Constant frequency loci, Constant damping ratio loci, Stability

Analysis of closed loop systems in the Z-Plane. Jury stablility test – Stability Analysis by use of the Bilinear Transformation and Routh Stability criterion.

DESIGN OF DISCRETE TIME CONTROL SYSTEM BY CONVENTIONAL METHODS: Transient and steady – State response Analysis – Design based on the frequency response method – Bilinear Transformation and Design procedure in the w-plane, Lead, Lag and Lead-Lag compensators and digital PID controllers.

UNIT – IV

STATE FEEDBACK CONTROLLERS AND OBSERVERS: Design of state feedback controller through pole placement – Necessary and sufficient conditions, Ackerman's formula. State Observers – Full order and Reduced order observers.

TEXT BOOKS:

1. Discrete-Time Control systems - K. Ogata, Pearson Education/PHI, 2nd Edition
2. Digital Control and State Variable Methods by M.Gopal, TMH

REFERENCES:

1. Digital Control Systems, Kuo, Oxford University Press, 2nd Edition, 2003.
2. Digital Control Engineering, M.Gopal

DIGITAL SYSTEM DESIGN

Subject Code: 17ECEPCD7

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to apply designing with programmable logic devices.

CO2.Implement transition count testing and test bridging faults.

CO3. Foster ability to machine identification and design of fault detection experiment.

CO4. Be able to evaluate finite state model and fundamental model.

17ECEPCD7: DIGITAL SYSTEM DESIGN

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit-I

Designing with Programmable Logic Devices

Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's– Using a One-hot state assignment,

State transition table- State assignment for FPGA's - Problem of Initial state assignment for One –Hot encoding - State Machine charts – Derivation of SM Charts – Realization of SM charts – Design Examples –Serial adder with Accumulator - Binary Multiplier – Signed Binary number multiplier (2's Complement multiplier) – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL.

Unit-II

Fault Modeling & Test Pattern Generation

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

Unit-III

Fault Diagnosis in Sequential Circuits

Circuit Test Approach, Transition Check Approach - State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

PLA Minimization and Testing

PLA Minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

Unit-IV

Minimization and Transformation of Sequential Machines

The Finite state Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines. Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

TEXT BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.
3. Logic Design Theory – N. N. Biswas, PHI

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd ed., 2001, TMH
2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.
3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

Embedded Real Time Operating Systems

Subject Code: 17ECEPCD8

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to evaluate process control signals and inter-process communication.

CO2. Implement periodic task model procedure constraints and data dependency.

CO3. Develop an understanding with inter-process communication and synchronization processes.

CO4.Foster ability to memory management task and state transition diagram.

17ECEPCD8: Embedded Real Time Operating Systems

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:		3 Hrs		Total Marks:	100

Unit – I

Introduction

Introduction to UNIX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec), Signals, Interprocess communication,(pipes, fifos, message queues, semaphores, shared memory)

Unit II

Real Time Systems:

Typical real time applications, Hard Vs Soft real-time systems, A reference model of Real Time Systems: Processors and Resources, Temporal Parameters of real Time Work load, Periodic task model precedence constraints and data dependency, functional parameters, Resource Parameters of jobs and parameters of resources.

Unit III

Scheduling & Inter-process Communication

Commonly used Approaches to Real Time Scheduling Clock Driven, Weighted Round Robin, Priority Driven, Dynamic Vs State Systems, Effective release time and Dead lines, Offline Vs Online Scheduling.

Inter-process Communication and Synchronization of Processes, Tasks and Threads- Multiple Process in an Application, Problem of Sharing data by multiple tasks & routines, Inter-process communication

Unit IV

Real Time Operating Systems & Programming Tools
Operating Systems Services, I/O Subsystems, RT & Embedded Systems OS, Interrupt Routine in RTOS Environment
Micro C/OS-II- Need of a well Tested & Debugged RTOs, Use of COS-II

VX Works & Case Studies

Memory managements task state transition diagram, pre-emptive priority, Scheduling context switches- semaphore- Binary mutex, counting watch dugs, I/O system

TEXT BOOKS:
1. Embedded Systems- Architecture, Programming and Design by Rajkamal, 2nd ed., 2008,TMH.
2. Real Time Systems- Jane W. S. Liu- PHI.
3. Real Time Systems- C.M.Krishna, KANG G. Shin, 1996, TMH
REFERENCES:
1. Advanced UNIX Programming, Richard Stevens
2. VX Works Programmers Guide

Internetworking

Subject Code: 17ECEPCD9

Course Outcomes:

By the end of the course the students will be able to:

CO1. Foster ability to network level interconnection and internet protocol address.

CO2. To understand fast recovery transmission and transition-oriented TCP.

CO3. Implement security in Internet firewalls and management components.

CO4. Be able to evaluate classical TCP improvements and time out freezing.

17ECEPCD9: Internetworking

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit -I:

Internetworking concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level Interconnection, Properties of thee Internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address: Classful Addressing: Introduction, Classful Addressing, Other Issues, Sub-netting and Super-netting

IP Address: Classless Addressing: - Variable length Blocks, Sub-netting, Address Allocation. Delivery, Forwarding, and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router. ***ARP and RARP:*** ARP, ARP Package, RARP.

Unit -II:

Internet Protocol (IP): Datagram, Fragmentation, Options, Checksum, IP V.6.

Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP Connection, State Transition Diagram, Flow Control, Error Control, Congestion Control, TCP Times.

Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP.

Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/ Fast Recovery, Transmission/ Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

Unit -III:

Unicast Routing Protocols (RIP, OSPF, and BGP: Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.
Multicasting and Multicast Routing Protocols: Unicast - Multicast- Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing: MOSPF, Multicast Distance Vector: DVMRP.

Unit -IV:

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space, and DNS in the internet.
Remote Login TELNET:- Concept, Network Virtual Terminal (NVT). ***File Transfer FTP and TFTP:*** File Transfer Protocol (FTP). ***Electronic Mail:*** SMTP and POP.
Network Management-SNMP: Concept, Management Components. World Wide Web- HTTP Architecture. Multimedia: Digitizing Audio and Video, Network security, security in the internet firewalls. Audio and Video Compression, Streaming Stored Audio/Video, Streaming Live Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP. Network Security, Security in the Internet, Firewalls.

TEXT BOOKS:

1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3 rd edition PHI

REFERENCES:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.

Micro Electromechanical Systems

Subject Code: 17ECEPCD10

Course Outcomes:

By the end of the course the students will be able to:

CO1. Implement broad response of micro electromechanical systems.

CO2. Be able to evaluate mechanical concepts like stress, strain and deflection curve.

CO3. Foster ability to application of Analog circuits like frequency converters and wave shaping.

CO4. Be able to design MEMS with optimum design technology.

17ECEPCD10: Micro Electromechanical Systems

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT –I

Introduction, basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT –II

Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, distributed force, distributed force, deflection curves for canti-levers- fixed beam. Electrostatic excitation – columbic force between the fixed and moving electrodes. Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – transient response of the MEMS.

UNIT – III

Two terminal MEMS - capacitance Vs voltage Curve – variable capacitor. Applications of variable capacitors. Two terminal MEM structures. Three terminal MEM structures – controlled variable capacitors – MEM as a switch and possible applications.

UNIT – IV

MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR<simple MEM configurations for flip-flops triggering applications to counters, converters.

Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS.

MEM Technologies: Silicon based MEMS- process flow – brief account of various processes and layers like fixed layer, moving layers spacers etc., and etching technologies.
Metal Based MEMS: Thin and thick film technologies for MEMS. Process flow and description of the processes. Status of MEMS in the current electronics scenario.

TEXT BOOKS:
1. MEMS Theory, Design and Technology - GABRIEL. M.Review, R.F.,2003, John wiley & Sons. .
2. Strength of Materials –Thimo Shenko, 2000, CBS publishers & Distributors.
3. MEMS and NEMS, Systems Devices; and Structures - Servey E.Lyshevski, 2002, CRC Press.
REFERENCE:
1. Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House, London.

Microcontrollers for Embedded system Design

Subject Code: 17ECEPCD11

Course Outcomes:

By the end of the course the students will be able to:

CO1 To acquire knowledge about microcontrollers embedded processors and their applications.

CO2 Foster ability to understand the internal architecture and interfacing of different peripheral devices with Microcontrollers.

CO3 Foster ability to write the programs for microcontroller.

CO4 Foster ability to understand the role of embedded systems in industry.

CO5 Foster ability to understand the design concept of embedded systems.

17ECEPCD11: Microcontrollers for Embedded system Design

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit – I:

Introduction to Embedded Systems

Overview of Embedded Systems, Processor Embedded into a system, Embedded Hardware Units and Devices in system, Embedded Software, Complex System Design, Design Process in Embedded System, Formalization of System Design, Classification of Embedded Systems.

Unit – II:

Microcontrollers and Processor Architecture & Interfacing

8051 Architecture, Input/Output Ports and Circuits, External Memory, Counters and Timers, PIC Controllers. Interfacing Processor (8051, PIC), Memory Interfacing, I/O Devices, Memory Controller and Memory arbitration Schemes.

Unit – III:

Embedded RISC Processors & Embedded System-on Chip Processor

PSOC (Programmable System-on-Chip) architectures, Continuous Timer blocks, Switched Capacitor blocks, I/O blocks, Digital blocks, Programming of PSOC, Embedded RISC

Processor architecture – ARM Processor architecture, Register Set, Modes of operation and overview of Instructions

Unit – IV:

Interrupts & Device Drivers

Exceptions and Interrupt handling Schemes – Context & Periods for Context Switching, Deadline & interrupt latency. Device driver using Interrupt Service Routine, Serial port Device Driver, Device drivers for Internal Programmable timing devices

Network Protocols

Serial communication protocols, Ethernet Protocol, SDMA, Channel & IDMA, External Bus Interface

TEXT BOOKS:

1. Embedded Systems - Architecture Programming and Design – Raj Kamal, 2nd ed., 2008,TMH.
2. PIC Microcontroller and Embedded Systems – Muhammad Ali Mazidi, Rolin D.Mckinaly, Danny Causy – PE.
3. Designers Guide to the Cypress PSOC – Robert Ashpy, 2005, Elsevier.

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.
2. ARM Systems Developers Guides- Design & Optimizing System Software - Andrew N. Sloss, Dominic Symes, Chris Wright, 2004, Elsevier.
3. Designing with PIC Microcontrollers- John B. Peatman, 1998, PH Inc.

Network Security & Cryptography

Subject Code: 17ECEPCD12

Course Outcomes:

By the end of the course the students will be able to:

CO1 To muster information security governance, and related legal and regulatory issues.
CO2 To be familiar with, how threats to an organization are discovered, analyzed, and dealt with.
CO3 To be familiar with network security threats and countermeasures.
CO4 To be familiar with advanced security issues and technologies (such as DDoS attack detection and containment, and anonymous communications) and have complete knowledge of different encryption algorithms used.

17ECEPCD12: Network Security & Cryptography

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT-I

Introduction: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internetwork security. Classical Techniques: Conventional Encryption model, Steganography, Classical Encryption Techniques**.**

UNIT-II

Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.
Conventional Encryption: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.
Public Key Cryptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT-III

Number theory: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.
Message authentication and Hash functions: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

Hash and Mac Algorithms: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. **Digital signatures and Authentication protocols**: Digital signatures, Authentication Protocols, Digital signature standards.
Authentication Applications: Kerberos, X.509 directory Authentication service.Electronic Mail Security: Pretty Good Privacy, S/MIME.

UNIT-IV

IP Security: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.
Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.
Intruders, Viruses and Worms : Intruders, Viruses and Related threats.
Fire Walls : Fire wall Design Principles, Trusted systems.

TEXT BOOK:

1. Cryptography and Network Security: Principles and Practice - William Stallings, 2000, PE.

REFERENCE:

1. Principles of Network and Systems Administration, Mark Burgess,John Wielly.

NEURAL NETWORKS AND FUZZY SYSTEMS

Subject Code: 17ECEPCD13

Course Outcomes:

By the end of the course the students will be able to:

CO1 Be able to define fuzzy sets using linguistic words and represent these sets by membership functions.

CO2 Become familiar with fuzzy relations and the properties of these relations.

CO3 Able to gain knowledge of architecture of various neural networks and their learning methods.

CO4 Be able to design fuzzy logic algorithms for specific use.

17ECEPCD13: NEURAL NETWORKS AND FUZZY SYSTEMS

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:	3 Hrs			Total Marks:	100

Unit – I

Biological neuron Vs Artificial neuron, structure and activation functions – Neural network
architectures-learning methods, stability and convergence.
Single layer networks -Mc Culloh- Pitts neuron model, Perceptron training and algorithm, Delta
learning, Widrow- Hoff learning rules, limitations, Adaline and modification.

UNIT II

Multilayer Networks-Architectures and Modelling, BP algorithm, radial basis functions.
Unsupervised learning-Winner take all learning, outstar learning, Counter propagation networks,
Self organizing networks-Kohonen,

UNIT III

Grossberg, Hamming NET, MAXNET, Hopfield networks, recurrent and
associative memory, BAM and ART architectures

Fuzzy sets and system – geometry of fuzzy sets – theorems – fuzzy and neural function estimators
– FAM system architectures – Uncertainty and estimation – Types of uncertainty –

UNIT IV

Measures of Fuzziness – Classical measures of uncertainty – Measures of dissonance – confession specificity – knowledge base defuzzification

Application to load forecasting, Load flow, Fault detection- unit commitments, LF control –
Economic dispatch, Neuro Fuzzy controllers

REFERENCE BOOKS:

1. Artificial Neural Networks – B.Yegna Narayana – PHI - 1st edition, 1999.
2. Neural Networks – Simon Haykin - Prentice Hall International Inc., 1999.
3. Neural Networks and Fuzzy System – Bart Kosko - 2nd edition, 2001.
4. Neural Network Fundamentals with Graphs, Algorithms & Applications – N. K. Bose and Liang – Mc Graw Hill, 1996.
5. Fuzzy logic with Fuzzy Applications – T.J.Ross – Mc Graw Hill Inc, 1997

HIGH SPEED NETWORKS

Subject Code: 17ECEPCD14

Course Outcomes:

By the end of the course the students will be able to:

CO1. Able to establish comparison between different transfer modes used in computer networks.

CO2. Foster ability to analyze the switching issues.

CO3. Evaluate various performance measures in switching.

CO4. To create understanding to establish comparison between ATM and MPLS, ATM and DSL Networks.

17ECEPCD14: HIGH SPEED NETWORKS

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:		3 Hrs		Total Marks:	100

UNIT I:

Overview of Computer Networks: Network Services, Network Elements, Basic Network Mechanisms. Transfer Modes: Introduction, Circuit Switching, Routing, Virtual Circuit Switching, Comparison of Transfer Modes.

Overview of ATM: Introduction, Motivation for ATM, Definition of ATM, Genesis of ATM, Precursor Technologies, Basic Principle of ATM, ISDN and B-ISDN, ISDN Channels, User Access, ISDN Protocols, Brief History of ISDN.

UNIT II:

ATM Protocol Reference Model: Introduction, Transmission Convergence (TC) Sub-layer, Physical Medium Dependent (PMD) Sub-layer, Physical Layer Standards for ATM. ATM Layer: ATM Cell Header Structure at UNI, ATM Cell Header Structure at NNI, ATM Layer Functions.

ATM Traffic Management: Introduction, ATM Traffic Contract Management, ATM Traffic Shaping, ATM Traffic Policing- Usage Parameter Control, ATM Priority Control, ATM Flow Control, ATM Congestion Control, Dynamics of TCP Traffic Over the ATM Networks.

ATM Addressing: Introduction, ATM End System Address (ASEA) Format, ATM Group Address, Acquiring ATM Address, ATM Name System (ANS).

ATM Signaling: Introduction, ATM Signaling, Protocol Stack, Signaling ATM Adaptation Layer (SAAL), UNI Signaling, ATM Point To Point Signaling, ATM Point To Multipoint Signaling.

ATM Routing: Introduction, Interim Inter-switch Protocol (IISP), PNNI Protocol, PNNI Routing Hierarchy.

UNIT III:

ATM Switching: Introduction, Components of a Typical Switch, Performance Measures in Switch Design, Switching Issues, Switching Architectures, Shared- Memory Architecture, Shared- Medium

Architecture, Space- Division Architecture, Switching in ATM. Interconnection Networks: Introduction, Banyan Networks- Properties, Crossbar Switch, Three Stage Class Networks, Rearrangeable Networks, Folding Algorithm, Benes Networks, Looping Algorithm, Bit- Allocation Algorithm.

UNIT IV:

ATM and MPLS Networks: Introduction, Overview of Multi-Protocol Label Switching (MPLS), ATM and MPLS.

Voice over ATM: Introduction, Technical Challenges, Carrying Voice over ATM.

ATM and DSL Networks: Introduction, Overview of Digital Subscriber Line (DSL), ATM and DSL, Voice over DSL (VoDSL), SONET/SDH: SONET/SDH Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks.

TEXT BOOKS:

1. TCP/IP Protocol Suite- Behrouz A. Forouzan, Third Edition, TMH
2. Internetworking with TCP/IP Comer 3 rd edition PHI

REFERENCES:

1. High performance TCP/IP Networking- Mahbub Hassan, Raj Jain, PHI, 2005
2. Data Communications & Networking – B.A. Forouzan – 2nd Edition – TMH
3. High Speed Networks and Internets- William Stallings, Pearson Education, 2002.
4. Data and Computer Communications, William Stallings, 7th Edition., PEI.

Micro Processor And Microcontrollers

Subject Code: 17ECEPCD15

Course Outcomes:

By the end of the course the students will be able to:

CO1. Compare between microprocessor and microcontroller.

CO2. Get familiar with the instruction set of various processors and 8051 controller.

CO3 Be able to distinguish between different modes of microprocessor.

CO4. Be able to implement programs in a microcontroller for optimum functioning

17ECEPCD15: Micro Processor And Microcontrollers

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

Unit I

8086/8088 processors : Introduction to 8086 Microprocessors, ,Architecture, Addressing modes, Instruction set, Register Organization, Assembler directives.

Hard ware description: Pindiagram signal description min & max modes, bus timing, ready & wait states, 8086 based micro computing system.
Special features & Related Programming : Stack structure of 8086, Memory segmentation, Interrupts, ISR, NMI, MI and interrupt Programming, Macros.

Unit II

Advanced Microprocessors: Intel 80386 programming model ,memory paging, Introduction to 80486, Introduction to Pentium Microprocessors and special Pentium pro features. Basic peripherals & Their Interfacing:-Memory Interfacing (DRAM) PPI-Modes of operation of 8255 ,Interfacing to ADC & DAC.

Unit III

Special Purpose of Programmable Peripheral Devices and Their interfacing :- Programmable interval timer , 8253 , PIC 8259A,display controller Programmable communication Interface 8251,USART and Exercises.

Unit IV

Microcontrollers : Introduction to Intel 8 bit &16 bit Microcontrollers, 8051-Architecture, Memory organization, Addressing Modes and exercises
Hardware description of 8051: Instruction formats ,Instruction sets, interrupt Structure & interrupt priorities, Port structures &Operation linear counter Functions ,different Modes of Operation and Programming examples.

TEXT BOOKS :-
1.”The Intel Microprocessors” Architecture Programming &Interfacing by Barry b Brey.
2.Advanceed Microprocessors by kenrith J Ayala , Thomson publishers.
3.Microcontrollers by kentrith J ayala,Thomson publishers.
Reference Books:-
1. Microprocessors & Interfacing Programming & Hard ware by DOUGLAS V.Hall
2. Microprocessors & Microcontrollers by Prof. C.R.Sarma

Robotics

Subject Code: 17ECEPCD16

Course Outcomes:

By the end of the course the students will be able to:

CO1. To gain complete knowledge of robotics and various robot systems including pumps, valves, solenoids.

CO2. Able to implement programming of various robots such as LEGO robot.

CO3.Compare various kinds of sensors according to their implementation in various applications.

CO4. Be able to write suitable algorithm for robot operation.

17ECEPCD16: Robotics

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:	3 Hrs			Total Marks:	100

Unit – I

Introduction & Basic Definitions

Introduction, Control Programs for Robots, Industry Applications of Robots, Pick and Place, Gantry and Arm type Robots in typical set-ups like Automobile Industry

Coordinate Systems : Cartesian, Cylindrical, Polar, and Revolute systems: Robot Positioning: Robor Arms; Axes, their ranges, offset and In-line Wrist: Roll, Pitch and Yaw, their meaning in Robotics

Unit-II

Mechanical Aspects

Kinematics, Inverse Kinematics, Motion planning and Mobile Mechanisms

Sensors and Applications

Range and Use of Sensors, Microswitches, Resistance Transducers, Piezo-electric, Infrared and Lasers

Applications of Sensors : Reed Switches, Ultrasonic, Barcode Readers and RFID

Unit-III

Robot Systems

Hydraulic and Electrical Systems including pumps, valves, solenoids, cylinders, stepper motors, Encoders and AC Motors

Unit-IV

Programming of Robots

Programming of Robots such as Lego Robots, Programming environment, Example Applications, Safety considerations

TEXT BOOKS:

1. Introduction to Robotics – P.J.Mckerrow, ISBN : 0201182408
2. Introduction to Robotics – S.Nikv, 2001, Prentice Hall,
3. Mechatronics and Robotics: Design & Applications – A.Mutanbara, 1999,CRC Press.

REFERENCES:

1. Robotics – K.S.Fu, R.C.Gonzalez and C.S.G.Lee, 2008, TMH.

Satellite Communications

Subject Code: 17ECEPCD17

Course Outcomes:

By the end of the course the students will be able to:

CO1. To acquire knowledge of satellite communication and factors effecting the seamless transmission of signals.

CO2. Comparative analysis of time division multiplexing and frequency division multiple access techniques.
CO3. Be able to design a satellite link and adjust parameters.
CO4. Be able to understand earth station design concept in details.

17ECEPCD17: Satellite Communications

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit-I

Communication Satellite: Orbit and Description
A Brief history of satellite Communication, Satellite Frequency Bands, Satellite Systems, Applications, Orbital Period and Velocity, effects of Orbital Inclination, Azimuth and Elevation, Coverage angle and slant Range, Eclipse, Orbital Perturbations, Placement of a Satellite in a Geo-Stationary orbit.

Unit-II

Satellite Sub-Systems
Attitude and Orbit Control system, TT&C subsystem, Attitude Control subsystem, Power systems, Communication subsystems, Satellite Antenna Equipment.
Satellite Link
Basic Transmission Theory, System Noise Temperature and G/T ratio, Basic Link Analysis, Interference Analysis, Design of satellite Links for a specified C/N, (With and without frequency Re-use).

Unit-III

Propagation effects

Introduction, Atmospheric Absorption, Cloud Attenuation, Tropospheric and Ionospeheric Scintillation and Low angle fading, Rain induced attenuation, rain induced cross polarization interference.

Frequency Division Multiple Access

FDM-FM-FDMA, Single channel per carrier, Companded FDM-FM-FDMA and SSB-AMFDMA,Intermodulation Products due to Amplitude Non-Linearity and Phase non-linearities, Optimized Carrier to Intermodulation plus noise ratio.

Unit-IV

Time Division Multiple Access

TDMA frame Structure, Burst Structure, Frame Efficiency, Super frame structure, Frame Acquisition and Synchronization, Burst Time Plan, TDMA timing, TDMA equipment and Advanced TDMA satellite systems.**Demand Assignment Multiple Access**

Types of Demand Assignments, DAMA characteristics, Real –Time Frame Configuration, DAMA interfaces, SCPC-DAMA, SPADE.

Satellite Packet Communications: Message Transmission by FDMA:M/G/1 Queue, Message Transmission by TDMA,PURE ALOHA-Satellite Packet Switching, Slotted Aloha, Packet Reservation,Tree Algorithm.

TEXT BOOKS:

1. Digital Satellite Communications-Tri.T.Ha, , 2nd Edition, 1990, Mc.Graw Hill.
2.Satellite Communications –Timothy Pratt, Charles Bostian, Jeremy Allnutt, 2nd Edition, 2003,John Wiley &Sons.

REFERENCES:

1. Satellite Communications-Dennis Roddy, 2nd Edition, 1996, Mc-Graw Hill.

Telecommunication Switching & Networks

Subject Code: 17ECEPCD18

Course Outcomes:

By the end of the course the students will be able to:

CO1. Gain thorough knowledge of switching techniques.

CO2.To create understanding of different switching networks.

CO3. To learn the basic switching fabric for implementation.

CO4. To gain knowledge of smart switching to avoid congestion in network.

17ECEPCD18: Telecommunication Switching & Networks

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT I:

Introduction: Evolution of Telecommunications, Simple Telephone Communication, Basics of Switching System, Manual Switching System, Major Telecommunication Networks.

Crossbar Switching: Principles of Common Control, Touch Tone Dial Telephone, Principles of Crossbar Switching, Crossbar Switch Configurations, Cross point Technology, Crossbar Exchange Organization.

UNIT II:

Electronic Space Division Switching: Stored Program Control, Centralized SPC, Distributed SPC, Software Architecture, Application Software, Enhanced Services, Two-Stage Networks, Three-Stage Networks, n- Stage Networks.

Time Division Switching: Basic Time Division Space Switching, Basic Time Division Time Switching, Time Multiplexed Space Switching, Time Multiplexed Time Switching, Combination Switching, Three- Stage Combination Switching, n- Stage Combination Switching.

UNIT III:

Telephone Networks: Subscriber Loop System, Switching Hierarchy and Routing, Transmission Plan, Transmission Systems, Numbering Plan, Charging Plan, Signaling Techniques, In-channel Signaling, Common Channel Signaling, Cellular Mobile Telephony

Signaling: Customer Line Signaling, Audio- Frequency Junctions and Trunk Circuits, FDM Carrier Systems, PCM Signaling, Inter- Register Signaling, Common- Channel Signaling Principles, CCITT Signaling System no.6, CCITT Signaling System no.7,Digital Customer Line Signaling.

Packet Switching: Statistical Multiplexing, Local- Area and Wide- Area Networks, Large-scale Networks, Broadband Networks.

UNIT IV:

Switching Networks: Single- Stage Networks, Gradings, Link Systems, Grades of service of link systems, Application of Graph Theory to link Systems, Use of Expansion, Call

Packing, Rearrangeable Networks, Strict- Sense non-blocking Networks, Sectionalized Switching Networks

Telecommunications Traffic: The Unit of Traffic, Congestion, Traffic Measurement, A Mathematical Model, Lost-call Systems, Queuing Systems.

Integrated Services Digital Network: Motivation for ISDN, New Services, Network and Protocol Architecture, Transmission Channels, User- Network Interfaces, Signaling, Numbering and Addressing, Service Characterization, Interworking, ISDN Standards, Expert Systems in ISDN, Broadband ISDN, Voice Data Integration.

TEXT BOOKS:

1. Telecommunication Switching Systems and Networks- Thiagarajan Viswanathan, 2000, PHI.
2. Telecommunications Switching, Traffic and Networks- J. E. Flood, 2006, Pearson Education.

REFERENCES:

1. Digital Telephony- J. Bellamy, 2nd Edition, 2001, John Wiley.
2. Data Communications and Networks- Achyut S. Godbole, 2004, TMH.
3. Principles of Communication Ststems- H. Taub & D. Schilling, 2nd Edition, 2003, TMH.
4. Data Communication & Networking- B. A. Forouzan, 3rd Edition, 2004, TMH.
5. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

VLSI Technology and Design

Subject Code: 17ECEPCD19

Course Outcomes:

By the end of the course the students will be able to:

CO1. Compare various MOS technologies.

CO2. Foster ability to simulate combinational logic circuits.

CO3. Perform design layouts for logic gates, combinational logic circuits and sequential circuits.

CO4.Be able to understand interworking of various gates and there combinations for testing.

17ECEPCD19: VLSI Technology and Design

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	**-**	**-**	**Examination:**	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT – I:

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends And Projections.

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: I_{ds}-V_{ds} relationships, Threshold Voltage V_t, G_m, G_{ds} and $\dot{A}_o$, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT – III:

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing.

UNIT –IV:

SEQUENTIAL SYSTEMS: Memory cells and Arrays, Clocking disciplines, Design, Power optimization, Design validation and testing.

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian. D, A.Pucknell, 2005, PHI.
2. Modern VLSI Design - Wayne Wolf, 3rd ed., 1997, Pearson Education.

REFERENCES:

1. Principals of CMOS VLSI Design – N.H.E Weste, K.Eshraghian, 2nd ed., Adisson Wesley.

Adhoc Wireless & Sensor Networks

Subject Code: 17ECEPCD20

Course Outcomes:

By the end of the course the students will be able to:

CO1. Compare between different wireless networks.

CO2. Evaluate various issues faced while designing routing protocols.

CO3. To comprehend various energy management methods for ad-hoc wireless networks.
CO4. Be able to design and maintain wireless network for various applications.

17ECEPCD20: Adhoc Wireless & Sensor Networks

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit-I:

Wireless LANS and PANS: Introduction, Fundamentals of WLANS, IEEE 802.11 Standard, HIPERLAN Standard, Bluetooth, Home RF.
Wireless Internet: Wireless Internet, Mobile IP, TCP in Wireless Domain, WAP, Optimizing Web Over Wireless.

Unit-II:

AD HOC Wireless Networks: Introduction, Issues in Ad Hoc Wireless Networks, AD Hoc Wireless Internet.
MAC Protocols for Ad Hoc Wireless Networks: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

Unit -III:

ROUTING PROTOCOLS: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.
TRANSPORT LAYER AND SECURITY PROTOCOLS: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks, Security in Ad Hoc Wireless Networks, Network Security Requirements, Issues and Challenges in Security Provisioning, Network Security Attacks, Key Management, Secure Routing in Ad Hoc Wireless Networks.

Unit – IV:

QUALITY OF SERVICE: Introduction, Issues and Challenges in Providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions, MAC Layer Solutions, Network Layer Solutions, QoS Frameworks for Ad Hoc Wireless Networks.

ENERGY MANAGEMENT: Introduction, Need for Energy Management in Ad Hoc Wireless Networks, Classification of Ad Hoc Wireless Networks, Battery Management Schemes, Transmission Power Management Schemes, System Power Management Schemes.

WIRELESS SENSOR NETWORKS: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press

REFERENCES:

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh ,1 ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

Algorithms for VLSI Design Automation

Subject Code: 17ECEPCD21

Course Outcomes:

By the end of the course the students will be able to:

CO1. Foster ability to design automation tools.

CO2. Able to understand dynamic programming and linear programming methods.

CO3. Implement design cycles for FPGAs and MCMs.

CO4. Implement two-level and high-level simulations.

17ECEPCD21: Algorithms for VLSI Design Automation

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	**-**	**-**	**Examination:**	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT I

PRELIMINARIES

Introduction to Design Methodologies, Design Automation tools, Algorithimic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING

Problems, Concepts and Algorithms.

MODELLING AND SIMULATION

Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT III

LOGIC SYNTHESIS AND VERIFICATION

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS

Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aqspects of Assignment problem, High-level Transformations.

UNIT IV

PHYSICAL DESIGN AUTOMATION OF FPGA'S

FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCM'S

MCM technologies, MCM phsical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

CMOS Analog & Mixed Signal Design

Subject Code: 17ECEPCD22

Course Outcomes:

By the end of the course the students will be able to:

CO1. Implement simple current mirrors and matching in MOSFET mirrors.

CO2. Compare different classes of amplifiers.

CO3. Evaluate performance of feedback amplifiers on basis of various parameters.

CO4. Implement Operational Amplifiers for various mathematical operations.

17ECEPCD22: CMOS Analog & Mixed Signal Design

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D	Marks of Internal:	20
3	-	-	Examination:	80
Duration of Exam: 3 Hrs			Total Marks:	100

CMOS ANALOG CIRCUITS:

UNIT – I:

Current Sources & Sinks: The cascode connection, sensitivity and temperature analysis, transient response, layout of simple Current Mirror, matching in MOSFET mirrors, other Current Sources/Sinks.

Voltage dividers, current source self-biasing, band gap voltage references, Beta-Multiplier Referenced Self-biasing.

UNIT – II:

Amplifiers: Gate Drain connected loads, Current Source Loads, Noise and Distortion, Class AB Amplifier.

Feedback Amplifiers: Feedback Equation, properties of negative feedback and amplifier design, feedback topologies, amplifiers employing the four types of feedback, Stability.

UNIT – III:

Differential Amplifiers: The Source Coupled pair, the Source Cross-Coupled pair, cascode loads, Wide-Swing Differential Amplifiers, **Operational Amplifiers:** Basic CMOS Op-Amp Design, Operational Trans conductance Amplifiers, Differential Output Op-Amp.

MIXED SIGNAL CIRCUITS:

UNIT – IV:

Non-Linear & Dynamic Analog Circuits: Basic CMOS Comparator Design, Adaptive Biasing,

Analog Multipliers, MOSFET Switch, Switched Capacitor circuits: Switched Capacitor Integrator, dynamic circuits.

Data Converter Architectures: Data Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures.

TEXT BOOKS:

1. CMOS Circuit Design, Layout and Simulation - Baker, Li, Boyce, 1st ed., TMH.

REFERENCES:

1. Analog Integrated Circuit Design – David A.Johns, Ken Martin, 1997, John-Wiley & Sons..
2. Design of Analog CMOS Circuits – B. Razavi, MGH, 2003, TMH.
3. Analog MOS ICs for Signal Processing – R.Gregorian, Gabor. C. Temes, John Wiley & Sons.

Design for Testability

Subject Code: 17ECEPCD23

Course Outcomes:

By the end of the course the students will be able to:

CO1. Implement modeling of digital circuits at different levels.

CO2. Foster ability to fault detection and redundancy.

CO3. Implement vector simulation.

CO4. Create understanding of different designs methodologies for testability.

17ECEPCD23: Design for Testability

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
Duration of Exam:	**3 Hrs**		**Examination:**	**80**
			Total Marks:	**100**

Unit – I

Introduction to Test and Design for Testability (DFT) Fundamentals

Modeling: Modeling Digital Circuits at Logic Level, register Level, and Structural Models. Levels of Modeling.

Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation

Unit – II

Fault Modeling: Logic Fault Models, Fault Detection and Redundancy, Fault equivalence and Fault Location. Single Stuck and Multiple Stuck- Fault Models, Fault Simulation Applications, General Techniques for Combinational Circuits.

Unit – III

Testing for Single Stuck Faults (SSF) – Automated Test Pattern Generation(ATPG/ATG) for SSFs in Combinational and Sequential Circuits, Functional Testing with Specific Fault Models, Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

Design for Testability – testability Trade-off's Techniques, Scan Architectures and Testing, Controllability and Absorbability, Generic Boundary Scan, Full Integrated Scan, Storage Cells foe Scan Design, Board level and System level approaches, Boundary Scans Standards, Compression Techniques – Different Techniques, Syndrome test and Signature analysis.

Unit – IV

Built-in Self test (BIST) – BIST Concepts and Test pattern Generation. Specific BIST Architectures –LOCST, STUMPS, CBIST, RTD, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Memory BIST (MBIST): Memory Test Architectures and Techniques, Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model, Memory Test requirements for MBIST, JTAG Testing Features.

TEXT BOOKS:

1. Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breur, Arthu D.Friedman, John Wiley & Sons.
2. Design for Test for Digital ICs & Embedded Core Systems – Alfred Crouch, 2008, PE.
3. Introduction to VLSI Testing – Robrt.J.Feugate J, Steven M.Mclntyre, Englehood Cliffs, 1988, Prentice Hall.

REFERENCE:

1. Essentials of Electronic Testing – M.L. Bushnell, Vishwani.D.Agarwal, Springer.

Detection and Estimation Theory

Subject Code: 17ECEPCD24

Course Outcomes:

By the end of the course the students will be able to:

CO1. Implement detection and estimation of signals.

CO2. To compare different estimation techniques.

CO3. To study different types of filters according to estimation theory.

CO4. To be able to design the transfer function of desired filter type.

17ECEPCD24: Detection and Estimation Theory

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:		3 Hrs		Total Marks:	100

Unit – I

Introduction, Simple Binary Hypothesis Tests, M-Hypothesis, Estimation Theory, Composite Hypothesis, General Gaussian Problem, Performance Bounds and Approximations, Sampling of Bandlimited Random Signals, Periodic random Processes, Spectral Decomposition, Vector Random Processes.

Unit – II

Detection & Estimation of Signals in White Gaussian Noise and Non-White Gaussian Noise, Signals with unwanted Parameters, Multiple Channels and Multiple Parameter, Linear & Non-Linear estimates, MLP & ML Estimates, Maximum Likelihood Estimate of Parameters of Linear Systems

Unit – III

Minimum Probability Error Criterion, Neyman-Pearson Criterion for Radar detection of Constant and variable amplitude signals, Matched Filters, Optimum formulation, Detection of Random Signals, Simple Problems there on with Multisample cases.

Unit – IV

Estimation of Continuous Waveforms: Derivation of Estimator Equations, A Lower Bound on the Mean Square Estimation Error, Multi dimensional Waveform Estimation, Nonrandom Waveform estimation.

Estimation of Time varying Signals – Kalman Filtering, Filtering Signals in Noise treatment, Restricted to two variable case only- simple Problems, Realizable Linear Filters, Kalman Bucy Filters, Fundamental role of Optimum Linear Filters.

TEXT BOOKS:

1. Detection, Estimation and Modulation Theory: Part – I – Harry L. Van Trees, 2001, John Wiley & Sons, USA.
2. Signal Processing : Discrete Spectral Analysis – Detection & Estimation – Mischa Schwartz, Leonard Shaw, 1975, McGrawHill.

REFERENCES :

1. Fundamentals of Statistical Signal Processing: Volume I Estimation Theory– Steven.M.Kay, Prentice Hall, USA, 1998.
2. Fundamentals of Statistical Signal Processing: Volume I Detection Theory– Steven.M.Kay, Prentice Hall, USA, 1998.
3. Introduction to Statistical Signal Processing with Applications - Srinath, Rajasekaran, Viswanathan, 2003, PHI.
4. Statistical Signal Processing: Detection, Estimation and Time Series Analysis – Louis L.Scharf, 1991, Addison Wesley.
5. Random Signals : Detection, Estimation and Data Analysis – K.Sam Shanmugam, Arthur M Breiphol, 1998, John Wiley & Sons.

Digital Signal Processors and Architectures

Subject Code: 17ECEPCD25

Course Outcomes:

By the end of the course the students will be able to:

CO1.Implement Discrete Fourier Transform and Fast Fourier Transforms.

CO2. Foster ability to understand different types of DSP devices.

CO3. Gathering knowledge and basic concepts of Interfacing of DSP devices.
CO4. Be able to design algorithm for implementation of desired device functionability.

17ECEPCD25: Digital Signal Processors and Architectures

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT III

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT IV

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA).

A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. 2000, S. Chand & Co.

REFERENCES

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkataramani and M. Bhaskar, 2002, TMH.
2. Digital Signal Processing – Jonatham Stein, 2005, John Wiley.

Hardware Software Co-Design

Subject Code: 17ECEPCD26

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to apply Co-Design modals & languages.

CO2. Implement target Architecture & system communication infrastructure.

CO3. Be able to evaluate Architecture for data dominating system & mixed systems.

CO4. Develop an understanding Embedded software development needs.

17ECEPCD26: Hardware Software Co-Design

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT –I

CO- DESIGN ISSUES

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

CO- SYNTHESIS ALGORITHMS :

Hardware software synthesis algorithms: hardware – software partitioning distributed system cosynthesis.

UNIT –II

PROTOTYPING AND EMULATION:

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

TARGET ARCHITECTURES:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES:
Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT – IV

DESIGN SPECIFICATION AND VERIFICATION:
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I System – level specification, design representation for system level synthesis, system level specification languages,

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II
Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS :

1. Hardware / software co- design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.
2. Hardware / software co- design Principles and Practice, 2002, kluwer academic publishers

Image & Video Processing

Subject Code: 17ECEPCD27

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to apply image transforms & wavelet transforms.

CO2. Be able to evaluate Arithmetic coding & run length coding.

CO3. Implement optical flow & global motion estimation.

CO4. Foster ability to application of motion estimation in video coding.

17ECEPCD27: Image & Video Processing

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT I

Fundamentals of Image Processing and Image Transforms

Basic steps of Image Processing System Sampling and Quantization of an image –
Basic relationship between pixels
Image Transforms: 2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT),
Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT II

Image Processing Techniques

Image Enhancement

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering,
Smoothing spatial filters, Sharpening spatial filters.
Frequency domain methods: Basics of filtering in frequency domain, image smoothing,
image sharpening, Selective filtering.

Image Segmentation

Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region
Based segmentation.

UNIT III

Image Compression

Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy,
Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding,

Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

Basic steps of Video Processing

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT V

2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Esimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXTBOOKS

1. Digital Image Processing – Gonzaleze and Woods, 3rd ed., Pearson.
2. Video processing and communication – Yao Wang, Joem Ostermann and Ya–quin

1. Digital Video Processing – M. Tekalp, Prentice Hall International

Mobile Computing Technologies

Subject Code: 17ECEPCD28

Course Outcomes:

By the end of the course the students will be able to:

CO1.Be able to evaluate GPRS & packet data network.

CO2. Be able to apply fundamentals of call processing.

CO3. Develop an understanding for security considerations in MIDP.

CO4.Be able to apply voice over internet protocol & convergence.

17ECEPCD28: Mobile Computing Technologies

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit – I

Introduction to Mobile Computing Architecture

Mobile Computing – Dialog Control – Networks – Middleware and Gateways – Application and Services – Developing Mobile Computing Applications – Security in Mobile Computing – Architecture for Mobile Computing – Three Tier Architecture – Design considerations for Mobile Computing – Mobile Computing through Internet – Making existing Applications Mobile Enabled.

CellularTechnologies: GSM, GPS, GPRS, CDMA and 3G

Bluetooth – Radio Frequency Identification – Wireless Broadband – Mobile IP – Internet Protocol Version 6 (IPv6) – Java Card – GSM Architecture – GSM Entities – Call Routing in GSM – PLMN Interfaces – GSM addresses and Identifiers – Network aspects in GSM – Authentication and Security – Mobile computing over SMS – GPRS and Packet Data Network – GPRS Network Architecture – GPRS Network Operations – Data Services in GPRS – Applications for GPRS – Limitations of GPRS – Spread Spectrum technology – Is-95 – CDMA Versus GSM – Wireless Data – Third Generation Networks – Applications on 3G

Unit – II

Wireless Application Protocol (WAP) and Wireless LAN

WAP – MMS – Wireless LAN Advantages – IEEE 802.11 Standards – Wireless LAN Architecture – Mobility in wireless LAN

Intelligent Networks and Interworking

Introduction – Fundamentals of Call processing – Intelligence in the Networks – SS#7 Signaling – IN Conceptual Model (INCM) – softswitch – Programmable Networks – Technologies and Interfaces for IN

Unit – III

Client Programming, Palm OS,Symbian OS, Win CE Architecture

Introduction – Moving beyond the Desktop – A Peek under the Hood: Hardware Overview – Mobile phones – PDA – Design Constraints in Applications for Handheld Devices – Palm OS architecture – Application Development – Multimedia – Symbian OS Architecture – Applications for Symbian, Different flavors of Windows CE -Windows CE Architecture

J2ME JAVA in the Handset – The Three-prong approach to JAVA Everywhere – JAVA 2 Micro Edition (J2ME) technology – Programming for CLDC – GUI in MIDP – UI Design Issues – Multimedia – Record Management System – Communication in MIDP – Security considerations in MIDP – Optional Packages

Unit – IV

Voice over Internet Protocol and Convergence

Voice over IP- H.323 Framework for Voice over IP – Session Initiation Protocol – Comparision between H.323 and SIP – Real Time protocols – Convergence Technologies – Call Routing – Voice over IP Applications – IP multimedia subsystem (IMS) – Mobile VoIP

Security Issues in Mobile Computing

Introduction – Information Security – Security Techniques and Algorithms – Security Protocols – Public Key Infrastructure – Trust – Security Models – Security frameworks for Mobile Environment

TEXT & REFERENCES BOOKS:

1. Mobile Computing – Technology, Applications and Service Creation – Asoke K Talukder, Roopa R Yavagal, 2009, TATA McGraw Hill
2. Mobile Communications – Jochen Schiller – 2nd Edition – Pearson Education
3. The CDMA 2000 System for Mobile Communications – Vieri Vaughi, Alexander Damn Jaonvic – Pearson
4. ADALESTEIN : Fundamentals of Mobile & Parvasive Computing, 2008, TMH

Optical Communications Technology

Subject Code: 17ECEPCD29

Course Outcomes:

By the end of the course the students will be able to:

CO1.Implement self-phase modulation & cross phase modulation.

CO2.Be able to apply optical switches & wavelength converters.

CO3. Develop an understanding with fiber non-linear & system design consideration.

CO4. Foster ability to dispersion limitation and compensation techniques.

17ECEPCD29: Optical Communications Technology

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

Unit – I

Signal propagation in Optical Fibers

Geometrical Optics approach and Wave Theory approach, Loss and Bandwidth, Chromatic Dispersion, Non Linear effects- Stimulated Brillouin and Stimulated Raman Scattering, Propagation in a Non-Linear Medium, Self Phase Modulation and Cross Phase Modulation, Four Wave Mixing, Principle of Solitons.

Unit – II

Fiber Optic Components for Communication & Networking

Couplers, Isolators and Circulators, Multiplexers, Bragg Gratings, Fabry-Perot Filters, Mach Zender Interferometers, Arrayed Waveguide Grating, Tunable Filters, High Channel Count Multiplexer Architectures, Optical Amplifiers, Direct and External Modulation Transmitters, Pump Sources for Amplifiers, Optical Switches and Wavelength Converters.

Unit – III

Modulation and Demodulation

Signal formats for Modulation, Subcarrier Modulation and Multiplexing, Optical Modulations – Duobinary, Single Side Band and Multilevel Schemes, Ideal and Practical receivers for Demodulation, Bit Error Rates, Timing Recovery and Equalization, Reed-Solomon Codes for Error Detection and Correction.

Unit – IV

Transmission System Engineering
System Model, Power Penalty in Transmitter and Receiver, Optical Amplifiers, Crosstalk and Reduction of Crosstalk, Cascaded Filters, Dispersion Limitations and Compensation Techniques.

Fiber Non-linearities and System Design Considerations
Limitation in High Speed and WDM Systems due to Non-linearities in Fibers, Wavelength Stabilization against Temperature Variations, Overall System Design considerations – Fiber Dispersion, Modulation, Non-Linear Effects, Wavelengths, All Optical Networks.

TEXT BOOKS:
1. Optical Networks: A Practical Perspective - Rajiv Ramaswami and Kumar N. Sivarajan, 2 ed., 2004, Elsevier Morgan Kaufmann Publishers (An Imprint of Elsevier).
2. Optical Fiber Communications – Gerd Keiser, 3 ed., 2000, McGraw Hill.
REFERENCES:
1. Optical Fiber Communications: Principles and Practice – John.M.Senior, 2 ed., 2000, PE.
2. Fiber Optics Communication – Harold Kolimbris, 2 ed., 2004, PEI
3. Optical Networks: Third Generation Transport Systems – Uyless Black, 2 ed., 2009, PEI
4. Optical Fiber Communications – Govind Agarwal, 2 ed., 2004, TMH.
5. Optical Fiber Communications and Its Applications – S.C.Gupta, 2004, PHI.

Optical Networks

Subject Code: 17ECEPCD30

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to evaluate optical line terminals and amplifiers.

CO2. Foster ability to optical layer services and interfacing.

CO3. Be able to apply multi-vendor inter-operability.

CO4. Develop an understanding with performance and fault management.

17ECEPCD30: Optical Networks

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

Unit – I:

Client Layers of Optical Networks

SONET / SDH – Multiplexing, Frame Structure, Physical Layer, Infrastructure, ATM – Functions, Adaptation layers, QoS, Flow Control Signaling and Routing, IP – Routing, QoS, MPLS, Storage Area Networks – ESCON, Fiber Channel, HIPPI, Gigabit Ethernet.

Unit - II:

WDM network Elements and Design

Optical Line Terminals and Amplifiers, Add/Drop Multiplexers, Optical Cross Connects, Cost trade-offs in Network Design, LTD and RWA Problems, Dimensioning – Wavelength Routing Networks, Statistical and Maximum Load Dimensioning Models.

Unit – III:

Network Control and Management

Network Management Functions, Optical Layer Services and Interfacing, Layers within Optical Layer, Multivendor Interoperability, Performance and Fault Management, Configuration Management, Optical Safety.

Unit – IV:

Network Survivability

Basic Concepts of Survivability, Protection in SONET/SDH Links and Rings, Protection in IP Networks, Optical Layer Protection – Service Classes, Protection Schemes, Interworking between Layers.

Access Networks and Photonic Packet Switching

Network Architecture, Enhanced HFC, FTTC, Photonic Packet Switching – OTDM, Synchronization, Header Processing, Buffering, Burst Switching, Test Beds.

TEXT BOOKS:

1. Optical Networks: A Practical Perspective - Rajiv Ramaswami and Kumar N. Sivarajan, 2 ed., 2004, Elsevier Morgan Kaufmann Publishers (An Imprint of Elsevier).
2. WDM Optical Networks: Concepts, Design and Algorithms – C. Siva Rama Murthy and Mohan Guruswamy 2 ed., 2003, PEI.
3. Optical Networks: Third Generation Transport Systems – Uyless Black, 2 ed., 2009, PEI.

REFERENCES:

1. Optical Fiber Communications: Principles and Practice – John.M.Senior, 2 ed., 2000, PE.
2. Fiber Optics Communication – Harold Kolimbris, 2 ed., 2004, PEI.
3. Networks – Timothy S. Ramteke, 2 ed., 2004, PEI.
4. Optical Fiber Communications – Govind Agarwal, 2 ed., 2004, TMH.
5. Optical Fiber Communications and Its Applications – S.C.Gupta, 2004, PHI.
6. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

Propagation Models for Wireless Communications

Subject Code: 17ECEPCD31

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to apply noise modeling and free space loss.

CO2. Implement ultra-wide bend indoor propagation an indoor link budget.

CO3. Develop an understanding with impact on coverage and local variability.

CO4. Foster ability to design a physical statistical model for built up areas.

17ECEPCD31: Propagation Models for Wireless Communications

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	P/D		Marks of Internal:	20
3	-	-	Examination:	80
Duration of Exam:	3 Hrs		Total Marks:	100

UNIT-I

Basic Propagation Models
Reflection, Refraction and Transmission, Rough surface scattering, Geometrical optics Principles.Diffraction – Principle and Single Knife Edge Diffraction. Definition of pathloss. Noise Modelling, Free Space Loss, Plane Earth loss

UNIT-II

Macrocells: Definition of parameters, Empirical Path Loss Models, Physical models, ITU-R models , comparison of models.
Empirical Models, Physical models, line-of-sight models, Non-line-of –sight models,
Picocells: Empirical models of propagation with in buildings, physical models of indoor propagation, Models of Propagation into buildings, ultra wide band indoor propagation, and Indoor link budgets

UNIT-III

Shadowing: Statistical charactrerisation, Physical basis for shadowing, Impact on coverage, location variability, correlated shadowing.
Fast fading: Narrow band fast fading channel, AWGN Channel, Narrow band fading channel, Rayleigh, Rice and Nakagani-m distribution, Wideband fast fading –Effect of wideband fading, wide band channel model and parameters, frequency domain effects and Bello functions.

UNIT-IV

Megacells: Shadowing and Fast fading,Empirical Narrowband models, Statistical Models, Physical- Statistical models for built-up areas, and over all mobile satellite channel model.

UNIT-VI

Overcoming Narrowband Fading : Space diversity, Polarization diversity, Time diversity, frequency diversity, and combining methods

Overcoming Wideband Fading : System modeling, Linear equalizers, Adaptive Equalizers, Non-Linear Equalizers, Rake receivers, and OFDM receivers.

TEXT BOOKS:

1. Antennas and Propagation for Wireless Communication Systems: Simon R. saunders, Alejandro Aragon-Zavala, 2nd ed. 2007, Wiley Student Edition.
2. Wireless Communication & Networks – Stallings, 2nd ed., 2009, Pearson Education.

REFERENCE

1. Wireless Communications – SAHA – 2nd Edition, 2009

Radar Signal Processing

Subject Code: 17ECEPCD32

Course Outcomes:

By the end of the course the students will be able to:

CO1.Be able to optimize radar range performance.

CO2. Develop an understanding with inverse probability receiver and sequential observations.

CO3. Foster ability to optimize wave forms for detection in clutter and family of radar wave forms.

CO4. Be able to evaluate phase coding techniques and maximal Length sequences.

17ECEPCD32: Radar Signal Processing

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
Duration of Exam:	**3 Hrs**		**Examination:**	**80**
			Total Marks:	**100**

Unit I

Introduction– Radar Block Diagram, Radar Equation, Information Available from Radar Echo. Review of Radar Range Performance– General Radar Range Equation, Radar Detection with Noise Jamming, Beacon and Repeater Equations, Bistatic Radar. Matched Filter Receiver – Impulse Response, Frequency Response Characteristic and its Derivation, Matched Filter and Correlation Function, Correlation Detection and Cross-Correlation Receiver. Efficiency of Non-Matched Filters, Matched Filter for Non-White Noise.

Unit II

Detection of Radar Signals in Noise: Detection Criteria – Neyman-Pearson Observer, Likelihood-Ratio Receiver, Inverse Probability Receiver, Sequential Observer. Detectors – Envelope Detector, Logarithmic Detector, I/Q Detector. Automatic Detection - CFAR Receiver, Cell Averaging CFAR Receiver, CFAR Loss, CFAR Uses in Radar. Radar Signal Management – Schematics, Component Parts, Resources and Constraints.

Unit III

Waveform Selection [3, 2] : Radar Ambiguity Function and Ambiguity Diagram – Principles and Properties; Specific Cases – Ideal Case, Single Pulse of Sine Wave, Periodic Pulse Train,

Single Linear FM Pulse, Noiselike Waveforms. Waveform Design Requirements. Optimum Waveforms for Detection in Clutter, Family of Radar Waveforms.

Unit IV

Pulse Compression in Radar Signals: Introduction, Significance, Types. Linear FM Pulse Compression – Block Diagram, Characteristics, Reduction of Time Sidelobes, Stretch Techniques, Generation and Decoding of FM Waveforms – Block Schematic and Characteristics of Passive System, Digital Compression, SAW Pulse Compression.

Phase Coding Techniques: Principles, Binary Phase Coding, Barker Codes, Maximal Length Sequences (MLS/LRS/PN), Block Diagram of a Phase Coded CW Radar.
Poly Phase Codes : Frank Codes, Costas Codes, Non-Linear FM Pulse Compression, Doppler Tolerant PC Waveforms – Short Pulse, Linear Period Modulation (LPM/HFM).
Sidelobe Reduction for Phase Coded PC Signals.

TEXT BOOKS :

1. Radar Handbook - M.I. Skolnik, 2nd ed., 1991, McGraw Hill.
2. Radar Design Principles : Signal Processing and The Environment - Fred E. Nathanson, 2nd ed., 1999, PHI.
3. Introduction to Radar Systems - M.I. Skolnik, 3rd ed., 2001, TMH.

REFERENCES :

1. Radar Principles - Peyton Z. Peebles, Jr., 2004, John Wiley.
2. Radar Signal Processing and Adaptive Systems - R. Nitzberg, 1999, Artech House.
3. Radar Design Principles - F.E. Nathanson, 1st ed., 1969, McGraw Hill.

RF Circuit Design

Subject Code: 17ECEPCD33

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to apply characteristics of amplifiers and configuration.

CO2. Implement low phase noise oscillation design.

CO3. Be able to evaluate lumped filter design and distributed filter design.

CO4. Develop and understanding with single and multi-port networks.

17ECEPCD33: RF Circuit Design

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT I:

INTRODUCTION TO RF ELECTRONICS

The Electromagnetic Spectrum, units and Physical Constants, Microwave bands – RF behavior of Passive components: Tuned resonant circuits, Vectors, Inductors and Capacitors - Voltage and Current in capacitor circuits – Tuned RF / IF Transformers.

UNIT II:

TRANSMISSION LINE ANALYSIS

Examples of transmission lines- Transmission line equations and Biasing- Micro Strip Transmission Lines- Special Termination Conditions- sourced and Loaded Transmission Lines.

SINGLE AND MULTIPORT NETWORKS

The Smith Chart, Interconnectivity networks, Network properties and Applications, Scattering Parameters.

UNIT III:

MATCHING AND BIASING NETWORKS

Impedance matching using discrete components – Micro strip line matching networks, Amplifier classes of Operation and Biasing networks.

RF PASSIVE & ACTIVE COMPONENTS

Filter Basics – Lumped filter design – Distributed Filter Design – Diplexer Filters- Crystal and Saw filters- Active Filters - Tunable filters – Power Combiners / Dividers – Directional Couplers – Hybrid Couplers – Isolators. RF Diodes – BJTs- FETs- HEMTs and Models.

UNIT IV:

RF TRANSISTOR AMPLIFIER DESIGN

Characteristics of Amplifiers - Amplifier Circuit Configurations, Amplifier Matching Basics, Distortion and noise products, Stability Considerations, Small Signal amplifier design, Power amplifier design, MMIC amplifiers, Broadband High Power multistage amplifiers, Low noise amplifiers, VGA Amplifiers.

OSCILLATORS

Oscillator basics, Low phase noise oscillator design, High frequency Oscillator configuration, LC Oscillators, VCOs, Crystal Oscillators, PLL Synthesizer, and Direct Digital Synthesizer.

TEXT BOOK:

1 RF circuit design: Theory and applications by Reinhold Ludwing, Pavel Bretchko. Pearson Education Asia Publication, New Delhi 2001.

REFERENCES:

1. Radio frequency and microwave electronics illustrated Mathew M. Radmangh, 2001,PE Asia Publication.
2. Secrets of RF Design by Joseph Carr., 3rd Edition, Tab Electronics.
3. Complete Wireless Design by Cotter W. Sawyer, 2nd Edition, Mc-Graw Hill.

Semiconductor Memory Design & Testing

Subject Code: 17ECEPCD34

Course Outcomes:

By the end of the course the students will be able to

CO1. Develop an understanding of Advance DRAM design and application specific DRAM.

CO2. Implement radiation hardening processes and design issues.

CO3. Be able to apply high density memory packaging for future directions.

CO4. Foster ability to application specific memory testing and BIST techniques for memory.

17ECEPCD34: Semiconductor Memory Design & Testing

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:		3 Hrs		Total Marks:	100

UNIT I:

Random Access Memory Technologies: SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, advanced DRAM design and architecture, Application specific DRAM

UNIT II:

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance:RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, nonvolatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT III:

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliabilty, Reliabilty Test Structures, Reliabilty Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening

techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT IV:

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu , 1st ed., Prentice Hall.

Speech Processing

Subject Code: 17ECEPCD35

Course Outcomes:

By the end of the course the students will be able to:

CO1. Develop an understanding with digital models and speech signals.

CO2. Implement homomorphism vocoders and pitch detection using LPC parameters.

CO3. Be able to apply single microphone approach and language models.

CO4. Foster ability to reorganization techniques and spoken verification systems.

17ECEPCD35: Speech Processing

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
Duration of Exam:	**3 Hrs**		**Examination:**	**80**
			Total Marks:	**100**

UNIT – I

Fundamentals of Digital Speech Processing:
Anatomy & Physiology of Speech Organs, The process of Speech Production, The Acoustic Theory of Speech Production, Digital models for speech signals.

Time Domain Models for Speech Processing
Introduction- Window considerations, Short time energy and average magnitude Short time average zero crossing rate ,Speech vs. silence discrimination using energy and zero crossing, Pitch period estimation using a parallel processing approach, The short time autocorrelation function, The short time average magnitude difference function, Pitch period estimation using the autocorrelation function.

UNIT – II

Linear predictive coding (LPC) analysis
Basic principles of Linear Predictive Analysis:The Autocorrelation Method, The Covariance Method,Solution of Lpc Equations: Cholesky Decomposition Solution for Covariance Method, Durbin's Recursive Solution for the AutoCorrelation Equations, Comparision between the Methods of Solution of the LPC Analysis Equations, Applications of LPC Parameters: Pitch Detection using LPC Parameters, Formant Analysis using LPC Parameters.

Homomorphic Speech Processing
Introduction, Homomorphic Systems for Convolution: Properties of the Complex Cepstrum, Computational Considerations,The Complex Cepstrum of Speech, Pitch Detection, Formant Estimation, The Homomorphic Vocoder.

UNIT – III

Speech enhancement:

-Nature of interfering sounds, Speech enhancment techniques: Single Microphone Approach : spectral substraction, Enhancement by re-synthesis, Comb filter, Wiener filter, Multimicrophone Approach.

Automatic speech recognition-

Basic pattern recognition approaches, Parametric represention of speech, Evaluating the similarity of speech patterns, Isolated digit Recognition System,. Contineous digit Recognition System

UNIT – IV

Hidden Markov Model (HMM) for Speech

Hidden markov model (HMM) for speech recognition,Viterbi algorithm,Training and testing using HMMS,Adapting to variability in speech(DTW), Language models.

Speaker recognition

Recognition techniques,Features that distinguish speakers, Speaker Recognition Systems: Speaker Verification System , Speaker Identification System.

TEXT BOOKS:

1. Digital processing of speech signals - L.R Rabiner and S.W.Schafer. Pearson Education.
2. Speech Communications : Human & Machine - Douglas O'Shaughnessy, 2nd ed., IEEE Press.
3. Digital processing of speech signals. L.R Rabinar and R W Schafer,1978, PHI.

REFERENCES:

1. Discrete Time Speech Signal Processing : principles and Practice - Thomas F. Quateri, PE.
2. Speech & Audio Signal Processing- Ben Gold & Nelson Morgan, 1 ed., Wiley.

System Modeling and Simulation

Subject Code: 17ECEPCD36

Course Outcomes:

By the end of the course the students will be able to:

CO1. Be able to evaluate simulation and single server queering system.

CO2. Implement generation of non-uniform and arbitrary random variants.

CO3. Be able to apply exponential distribution and simulating a poison processor.

CO4. Develop an understanding of comparison of simulation packages with programming languages.

17ECEPCD36: System Modeling and Simulation

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

Unit – I

Basic Simulation Modeling, Systems, Models and Simulation, Nature of Systems, event Driven Models, Simulation of Single Server Queuing System, event Driven Models, Characterizing Systems, Simulation Diagrams.

Unit – II

Stochastic generators

Uniformly Distributed Random Numbers, Statistical Properties of U[0,1] generators, Generation of Non-Uniform and Arbitrary Random Variates, Random processes, Characterizing and Generating Random Processes, White Noise.

Modelling Time Driven Systems: Modelling Input Signals, Discrete and Distributed Delays, System Integration, Linear Systems.

Exogenous Signals and Events: Disturbance Signals, State Machines, Petri Nets and their Analysis, System Encapsulation.

Unit – III

Markov Process

Probabilistic Models, Discrete Time Markov Processes, Random Walks, Poisson Processes, Exponential Distribution, Simulating a Poisson Process, Continuous Time Markov Process

Event Driven Models: Simulation Diagrams, Queuing Theory, M/M/I Queues, Simulating Queuing Systems, Finite Capacity Queues, Multiple Servers, M/M/C Queues.

System Optimization

System Identification, Searches, Alpha / Beta trackers, Multidimensional Optimization, Modeling and Simulation Methodology.

Unit – IV

Simulation Software and Building Simulation Models

Comparison of Simulation Packages with Programming Languages, Classification of Simulation Software, Desirable software features, General Purpose Simulation Packages- Arena, Extend; Guide lines for determining the level of Model detail, Techniques for increasing Model Viability and credibility.

TEXT BOOKS:

1. System Modelling and Simulation: An Introduction – Frank L. Severance, 2001,John Wiley&Sons.
2. Simulation Modelling and Analysis - Averill M.Law, W.David Kelton, , 3 ed., 2003, TMH.

REFERENCE:

1. Systems Simulation-Geoffery Gordan, PHI.

System On Chip Architecture

Subject Code: 17ECEPCD37

Course Outcomes:

By the end of the course the students will be able to:

CO1. Foster ability to design low power consumption and ARM-coprocessor interface.

CO2. Be able to apply co-processor instruction and architectural support for high level language.

CO3. Implement context switching input and output.

CO4. Develop an understanding of abstraction in software design and architecture inheritance.

17ECEPCD37: System On Chip Architecture

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	**-**	**-**	**Examination:**	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

UNIT I:

Introduction to Processor Design: Abstraction in Hardware Design, MUO a simple processor ,Processor design trade off, Design for low power consumption

ARM Processor as System-on-Chip: Acorn RISC Machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface

UNIT II:

ARM Assembly Language Programming: ARM instruction types – data transfer, data processing and control flow instructions – ARM instruction set – Co-processor instructions

Architectural Support for High Level Language: Data types – abstraction in Software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory

UNIT III:

Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache design-an example – memory management

Architectural Support for System Development: Advanced Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware system prototyping tools – Armulator – Debug architecture

UNIT IV:

Architectural Support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU Architecture – Synchronization – Context Switching input and output

TEXT BOOKS:

1. ARM System on Chip Architecture – Steve Furber – 2nd ed., 2000, Addison Wesley Professional.
2. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st ed., 2004, Springer

REFERENCES:

1. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
2. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001,Kluwer Academic Publishers.

VLSI Signal Processing

Subject Code: 17ECEPCD38

Course Outcomes:

By the end of the course the students will be able to:

CO1. To acquire knowledge of DSP algorithm benefits and pipelining and parallel processing for low power.

CO2. To compare register minimization techniques in folded and unfolded architecture.

CO3. To evaluate programmable digital signal processors for mobile and wireless communication.

CO4. To implement design of fast convolution algorithm by inspection.

17ECEPCD38: VLSI Signal Processing

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT I:

Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT-II

Folding and Unfolding:

Folding : Introduction -Folding Transform - Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

Unfolding: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

UNIT III:

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain Delays

UNIT IV:

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

Low Power Design: Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches

Programmable DSP : Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing

TEXT BOOKS:

1. VLSI Digital Signal Processing- System Design and Implementation – Keshab K. Parthi, 1998, Wiley Inter Science.
2. VLSI and Modern Signal processing – Kung S. Y, H. J. While House, T. Kailath, 1985, Prentice Hall.

REFERENCES:

1. Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing – Jose E. France, Yannis Tsividis, 1994, Prentice Hall.
2. VLSI Digital Signal Processing – Medisetti V. K ,1995, IEEE Press (NY), USA.

Voice over Internet Protocol

Subject Code: 17ECEPCD39

Course Outcomes:

By the end of the course the students will be able to:

CO1. Compare Transmission Control Protocol (TCP) and User Datagram Protocol (UDP).

CO2. Implement SDP with SIP.

CO3. Able to understand different protocols for Quality of Service (QoS).

CO4. Get familiar with SS7 protocol suite and Internetworking soft switch and SS7.

17ECEPCD39: Voice over Internet Protocol

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:	3 Hrs			Total Marks:	100

Unit – I:

Overview of IP Protocol Suite

The Internet Protocol, The Transmission Control Protocol(TCP), The User Datagram Protocol (UDP), The Real-time Transport Protocol (RTP), IP multicast, IP version 6 (IP v6), Interworking IPv4 and IPv6, The VoIP Market, VoIP Challenges.

Unit - II:

H.323 and H.245 Standards

The H.323 Architecture, Call Signaling-Call Scenarios, H.245 Control Signaling Conference calls- The Decomposed Gateway.

The Session Initiation Protocol (SIP)

SIP architecture- Overview of SIP Messaging Syntax- Examples of SIP Message sequences- Redirect Servers- Proxy Servers. The Session Description Protocol (SDP)- Usage of SDP With SIP.

Unit-III:

Quality of Service (QoS)

Need for QOS – End-to-end QoS, Overview of QOS solutions- The Resource reservation Protocol(RSVP)- Diffserv- The Diffserv Architecture- Multi-protocol Label Switching (

MPLS)-The MPLS Architecture- MPLS Traffic Engineering- Label Distribution Protocols and Constraint- Based Routing.

Unit-IV:

VoIP and SS7

The SS7 Protocol Suite- The Message Transfer Part (MTP), ISDN User Part (ISUP) and Signaling Connection Control Part (SCCP), SS7 Network Architecture- Signaling Points(SPs)-Single Transfer Point (STP), - Service Control Point(SCP)- Message Signal Units (MSUs)- SS7 Addressing, ISUP, Performance Requirements for SS7, Sigtran- Sigtran Architecture- SCTPM3UA
Operation- M2UA Operation- M2PA Operation- Interworking SS7 and VoIP Architectures- Interworking Soft switch and SS7- Interworking H.323 and SS7.

TEXT BOOKS:

1. Carrier Grade Voice over IP – Daniel Collins, 2nd ed., TMH.

Wireless Communications & Networks

Subject Code: 17ECEPCD40

Course Outcomes:

By the end of the course the students will be able to:

CO1. To acquire knowledge of fundamentals related to wireless communication.

CO2. To establish basic understanding of multiple access techniques.

CO3. To evaluate performance of various switching networks.

CO4. To compare mobile data networks and ad-hoc wireless networks.

17ECEPCD40: Wireless Communications & Networks

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		Marks of Internal:	20
3	-	-		Examination:	80
Duration of Exam:		3 Hrs		Total Marks:	100

UNIT I:

Wireless Communications & System Fundamentals:
Introduction to wireless communications systems, examples, comparisons & trends, Cellular concepts-frequency reuse, strategies, interference & system capacity, trucking & grade of service, improving coverage &capacity in cellular systems.

UNIT II

Multiple Access Techniques for Wireless Communication:
FDMA, TDMA, SSMA (FHMA/CDMA/Hybrid techniques), SDMA technique (AS applicable to wireless communications).Packet radio access-protocols, CSMA protocols, reservation protocols, capture effect in packet radio, capacity of cellular systems.

Wireless Networking:
Introduction, differences in wireless & fixed telephone networks, traffic routing in wireless networks –circuit switching, packet switching X.25 protocol.
Wireless data services – cellular digital packet data (CDPD), advanced radio data information systems, RAM mobile data (RMD). Common channel signaling (CCS), ISDN-Broad band ISDN & ATM, Signaling System no .7 (SS7)-protocols, network services part, user part, signaling traffic, services & performance

UNIT III:

Mobile IP and Wireless Application Protocol: Mobile IP Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, overview, WML scripts, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol.

Wireless LAN Technology

Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs, IEEE 802 protocol Architecture, IEEE802 architecture and services, 802.11 medium access control, 802.11 physical layer.

UNIT IV:

Mobile Data Networks: Introduction, Data oriented CDPD Network, GPRS and higher data rates, Short messaging service in GSM, Mobile application protocol.

Ad-hoc Wireless Networks: Cellular and Adhoc wireless networks, applications, MAC protocols, Routing, Multicasting, Transport layer Protocols, quality of service browsining, deployment considerations, Adhoc wireless Internet

TEXT BOOKS

1. Wireless Communication and Networking – William Stallings, 2003, PHI.
2. Wireless Communications, Principles, Practice-Theodore, S.Rappaport, 2nd Edn. 2002, PHI.
3. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, 2002, PE

1. Wireless Digital Communications – Kamilo Feher, 1999, PHI.
2. Telecommunication System Engineering – Roger L. Freeman, 4/ed., Wiley-Interscience, John Wiley & Sons, 2004.

Transform Techniques

Subject Code: 17ECEPCD41

Course Outcomes:

By the end of the course the students will be able to:

CO1. To acquire knowledge about different kinds of transforms.

CO2. To understand basics of decimation and interpolation in time and frequency domain.

CO3. To implement various types of multidimensional wavelets.

CO4. To study implementation of DCT, DNT and fractal signal analysis.

17ECEPCD41: Transform Techniques

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT I:

Review of Transforms: Signal spaces, concept of convergence, Hilbert spaces for energy signals, Fourier basis, FT-failure of FT-need for time-frequency analysis, spectrogram plot-phase space plot in time-frequency plane, Continuous FT, DTFT, Discrete Fourier Series and Transforms, Z-Transform, relation between CFT-DTFT, DTFT-DFS,DFS-DFT, DCT(1D&2D), Walsh, Hadamard, Haar, Slant, KLT,Hilbert Transforms – definition, properties and applications

UNIT II:

CWT & MRA: Time-frequency limitations, tiling of time-frequency plane for STFT, Heisenberg uncertainty principle, Short time Fourier Transform (STFT) analysis, short comings of STFT, Need for wavelets- Wavelet Basis- Concept of Scale and its relation with frequebcy , Continuous time wavelet Transform Equation- Series Expansion using Wavelets- CWT- Need for scaling Function- Multi resolution analysis, Tiling of time scale plane for CWT. Important Wavelets : Haar, Mexican Hat Meyer, Shannon, Daubechies.

UNIT III:

Multirate Systems , Filter Banks and DWT.

Basics of Decimation and Interpolation in time & frequency domains, Two-channel Filter bank, Perfect Reconstruction Condition, Relation ship between Filter Banks and Wavelet basis, DWT Filter Banks For Daubechies Wavelet Function

UNIT IV:

Special Topics: Wavelet Packet Transform Multidimensional Wavelets, Bi-orthogonal basis-Bsplines, Lifting Scheme of Wavelet Generation, Multi Wavelets

Applications of Transforms

Signal Denoising, Subband Coding of Speech and Music, Signal Compression - Use of DCT, DWT,KLT, 2-D DWT, Fractal Signal Analysis.

Text Books:

1. "Fundamentals of Wavelets- Theory, Algorithms and Applications", Jaideva C Goswami, Andrew K Chan, John Wiley & Sons, Inc, Singapore, 1999.
2. Wavelet Transforms-Introduction theory and applications-Raghuveer M.Rao and Ajit S. Bopardikar, Pearson edu, Asia, New Delhi, 2003.
3. "Insight into Wavelets from Theory to practice ", Soman.K.P, Ramachandran. K.I, Printice Hall India, First Edition, 2004.

Reference Books:

1. "Wavelets and sub-band coding", Vetterli M. Kovacevic, PJI, 1995.
2. "Introduction to Wavelets and Wavelet Transforms", C. Sydney Burrus, PHI, First Edition, 1997.
3. "A Wavelet Tour of Signal Processing", Stephen G. Mallat,. Academic Press, Second Edition,

EMI/EMC

Subject Code: 17ECEPCD42

Course Outcomes:

By the end of the course the students will be able to:

CO1. To acquire knowledge of various open area test sites and measurements.

CO2. To get familiar with EMI detectors and measurements.

CO3. To understand various types of filters and their designing.
CO4.Be able to implement shielding and grounding of various types.

17ECEPCD42: EMI/EMC

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT-I.

Introduction, Natural and Nuclear sources of EMI/EMC:
Electromagnetic environment, History, Concepts, Practical experiences and concerns, frequency spectrum conservations. An overview of EMI/EMC, Natural and Nuclear sources of EMI.

UNIT-II.

EMI from apparatus, circuits and open area test sites:
Electromagnetic emissions, noise from relays and switches, non-linearities in circuits, passive intermodulation, cross talk in interference (EMI). Open area test sites and measurements.

UNIT-III.

Radiated and conducted interference measurements and ESD:
Anechoic chamber, TEM cell, GH TEM cell, characterization of conduction currents/voltages, conducted EM noise on power lines, conducted EMI from equipment, Immunity to conducted. EMI detectors and measurements. ESD, Electrical fast transients/bursts, electrical surges.

UNIT-IV.

Grounding, shielding, bonding and EMI filters:
Principles and types of grounding, shielding and bonding, characterization of filters, power lines filter design.
Cables, connectors, components and EMC standards:
EMI suppression cables, EMC connectors, EMC gaskets, Isolation transformers, optoisolators, National/International EMC standards.
Text Book:

1. Engineering Electromagnetic Compatibility by Dr. V.P. Kodali, IEEE
Publication, Printed in India by S. Chand & Co. Ltd., New Delhi, 2000.
2. Electromagnetic Interference and Compatibility IMPACT series, IIT-Delhi, Modules 1-9.

References:

1. Introduction to Electromagnetic Compatibility, Ny, John Wiley, 1992, by C.R. Pal.

Microwave Circuits & Microwave Integrated Circuits

Subject Code: 17ECEPCD43

Course Outcomes:

By the end of the course the students will be able to:

CO1. To acquire knowledge of fundamentals of microwave circuits.

CO2. To understand various types of plane tees and relationship among different parameters.

CO3. To analyze characteristic parameters of strip line and micro-strip lines.

CO4. To implement fabrication of lumped elements of MIC design.

17ECEPCD43: Microwave Circuits & Microwave Integrated Circuits

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam: 3 Hrs			**Total Marks:**	**100**

Unit-I:

Introduction to Microwave circuit concepts: one port junction, terminal voltages & currents in multi port junctions, Poynting's Energy Theorem, Normalized waves and scattering matrix. Properties of [S] matrix.

Unit-II:

Relation between [S], [Z] and [Y] parameters, Wave amplitude transmission matrix [A], relation between [A] and [S], [S] matrix of magic T, E and H plane Tees, directional coupler, Application of Hybrid junction and magic tee.

Unit-III:

MIC technology – Thick film & thin film technology, Hybrid MICs
Analysis of strip line & micro-strip line, Method of conformal transformation, Characteristic parameters of strip line and micro-strip lines, Micro-strip circuit design, Impedance transformers, Lumped constant micro-strip circuits.

Unit-IV:

Lumped elements for MIC's design & fabrication of lumped elements, circuits using lumped elements.
Design of Micro-strip circuits - high power & low power circuits.

References:

1. Altman, JL., Microwave Circuits, D. Van Nostrand Co., Inc., 1964.
2. Microwave Integrated Circuits by D. Van Nostrand Co. Inc.
3. Foundations for Microwave Engineering, McGraw Hill 2nd edn, 1992.

4. Microwave Integrated Circuits by K.G. Gupta & Amarjit Singh.
5. Advances in Microwave by Leo young.

GLOBAL POSITIONING SYSTEMS

Subject Code: 17ECEPCD44

Course Outcomes:

By the end of the course the students will be able to:

CO1. To implement position estimation with pseudo range measurements.

CO2. To evaluate the performance of GPS by studying different possible errors.

CO3. To evaluate hardware and software improvements for GPS.

CO4. To acquire knowledge of GPS applications and GPS integration.

17ECEPCD44: GLOBAL POSITIONING SYSTEMS

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT I

GPS Principles: History of Navigation, GPS Constellation, Principle of operation, GPS Orbits, Orbital mechanics and satellite position determination, Time references, Various DOPs, signal structure, Code and carrier phase measurements, position estimation with pseudorange measurements.

UNIT II

Error in GPS: Satellite and receiver clock errors, Ephemeris error, Atmospheric errors, Receiver measurement noise and UERE. Error budget.
Datum coordinate systems: Geometry of ellipsoid, geodetic reference system. Geoid, Ellipsoid, Global and Regional datums WGS-84, IGS, ECI, ECEF.

UNIT III

GPS Modernization and DGPS: Future GPS satellites, new signals and their benefits, hardware and Software improvements. Principle and operation of DGPS. Code-based and carrier based DGPS Techniques, DGPS errors.

UNIT IV

GPS Augmentation systems: Relative advantages of SBAS and GBAS, Wide area augmentation system (WAAS) architecture, Link budget. GAGAN, EGNOS and MSAS. Local area augmentation system (LAAS) concept.
Applications of GPS: GPS applications, GPS integration – GPS/GIS, GPS/INS, GPS/pseudolite, GPS/cellular. Other satellite navigation constellations GLONASS and Galileo System.

Text Books

1. Pratap Misra and Per Enge, "Global Positioning System Signals, Measurements, and Performance," Ganga-Jamuna Press, Massachusetts, 2001.
2. B.Hofmann-Wellenhof, H.Lichtenegger, and J.Collins, "GPS Theory and Practice," Springer Wien, New York, 2000.
3. Ahmed El-Rabbany, "Introduction to GPS," Artech House, Boston, 2002.

Suggested Reading

1. Bradford W. Parkinson and James J. Spilker, "Global Positioning System: Theory and Applications," Volume II, American Institute of Aeronautics and Astronautics, Inc., Washington, 1996.
2. Elliot D.Kaplan, "Understanding GPS Principles and Applications," Artech House, Boston, 1996.
3. A.Leick, "GPS Satellite Surveying", John Wiley and sons, 1990.

MICROWAVE ANTENNAS

Subject Code: 17ECEPCD45

COurse Outcomes:

By the end of the course the students will be able to:

CO1. Learning of all the parameters of Antenna.

CO2. To understand all types of Reflectors Antennas and able to establish comparison among them.

CO3. Foster ability to evaluate antenna arrays.

CO4. To evaluate advantages of disadvantages of micro strip radiators.

17ECEPCD45: MICROWAVE ANTENNAS

Note: Total 9 questions are to be set by the examiner/teacher covering the entire syllabus uniformly the question paper, question no 1 will be set up from all the four sections/units and of short answer type. A candidate is required to attempt any five questions at least one question from each unit. Question no. 1 is Compulsory. All questions shall carry equal marks.

L	T	P/D		
3	-	-	**Marks of Internal:**	**20**
			Examination:	**80**
Duration of Exam:	**3 Hrs**		**Total Marks:**	**100**

UNIT-I

Antenna Parameters: Radiation Patterns, Radiation Power Density, Radiation Intensity, Gain, Antenna Efficiency, Bandwidth, Polarization, Input Impedance, Antenna Radiation Efficiency, Antenna as an Aperture, Directivity and maximum Aperture, Friis Transmission Equation, Antenna Temperature.

UNIT-II

Reflector Antennas: Plane Reflector, Corner Reflector, 90_o Corner Reflector, Other Corner Reflectors, Parabolic Reflector, Front-Fed Parabolic Reflector, Cassegrain Reflectors, Lens Antennas, Lenses with $n>1$, Lenses with $n<1$, Lenses with Variable Index of Refraction.

UNIT-III

Antenna Arrays: Introduction, Two Element Array, N-Element Linear Array- Uniform amplitude and Spacing, Broadside Array, Ordinary End-Fire Array, Phased Array, Hansen-Woodyard End-Fire Array, N-Element Linear Array- Directivity, Nonuniform Amplitude, Binomial Array-Design equations.

UNIT-IV

Microstrip Radiators: Definition of microstrip antenna, advantages and disadvantages of microstrip antennas, applications, Radiation mechanism and Radiation fields of microstrip antennas, excitation techniques.

Rectangular microstrip patch antennas: Introduction, Analysis of Rectangular patch radiators, The vector potential approach, Dyadic Green's Function Techniques, the cavity model, Model Expansion Model, the transmission line model, Bandwidth Enhancement Techniques.

Suggested reading:

1. J.D. Kraus, Antennas, MC Graw-Hill, ISE, 1988.
2. Constantine A. Balanis, "Antenna theory analysis and Design", John Wiley.
3. J.J. Bahl and Bhartia, "Microstrip antennas", Artech House, 1982.

References:

1. Samuel Silver, "Microwave Antenna – Theory and Design", IEE Press, London 1984.
2. James J. Hall, P.S. Wood, Microstrip Antenna – Theory and Design, 1981.